Page v, line 19

13 Operational-Amplifier Circuits

Page xx, beginning with 10th line from bottom

6. Streamlined Presentation of Frequency Response. While keeping the treatment of frequency response all together, the chapter has been rewritten to streamline its flow, and simplify and clarify the presentation.

7. Clearer and Simplified Study of Feedback. The feedback chapter has been rewritten to improve, simplify, and clarify the presentaton of this key subject.

Page xxi, second line from bottom

- Appendix F: s-Domain Analysis: Poles, Zeros, and Bode Plots

Page 169, line 1

Table 3.1 Summary of Important Semiconductor Equations

Page 322

Figure correction: see end of document.

Page 453 – Table 7.5, third line from bottom

[a] For the interpretation of $R_{in}, A_{vo},$, and R_o refer to Fig. 7.34(b).

Page 495, right-hand column, line 28

Problem D *7.108 It is required to design the bias circuit of Fig. 7.52(a) for a BJT whose nominal $\beta = 100$.

Page 510, seventh line from bottom

(For a discussion of Moore's law and device scaling, see Section 15.1.)

Page 549, line 8

We will demonstrate this point in Section 10.5.

Page 554, line 17

…for as we shall see in Section 10.5…

Page 554, line 21

However, as will be seen in Section 10.5…

Page 580, left-hand column, sixth line from bottom

…neglect r_o.)

Page 580, right-hand column, eighth line from bottom

…Table K.1 in Appendix K,…

Page 580, right-hand column third line from bottom

…Table K.1 in Appendix K…

Page 632, Example 9.4, line 9

$$g_m = \sqrt{\mu_n C_{ox)} (\frac{W}{L}) V_{OV}}$$

Page 632, Example 9.4, lines 10-11

It can be seen that an error of 2% in W/L will result in an error in g_m of 2% . That is, the 2% mismatch in the W/L ratios of Q_1 and Q_2 will result in a 2% mismatch in their g_m values. …

Page 632, Example 9.4, line 15

$10^5 = (2 g_m R_{SS})/0.02$

Page 632, Example 9.4, line 20

$R_{SS} = 1\ \text{M}\Omega$.

Page 632, Example 9.4, line 22

$r_o = R_{SS} = 1\ \text{M}\Omega$.

Page 633, line 2

$\frac{V_A}{I} = 1\ \text{M}\Omega$.

Page 633, line 4

$V_A = 200\ \text{V}$

Page 633, line 6

$L = 40\ \mu\text{m}$

Page 633, lines 13-14

$1000 = 2 \text{ x } r_o^2$

$r_o = 22.36\ \text{k}\Omega$

Page 633, line 17

$V_A = 4.47\ \text{V}$

Page 633, line 19

$L = \frac{4.47}{V_A'} = \frac{4.47}{5} = 0.89$

Page 697, Line 19

Our study of transistor amplifiers in Chapters 7 through 9…

Page 705, footnote line 1

[1]The derivation of this expression is simple and is given in Chapter **7**…

Page 707, line 16

$$f_L \simeq \frac{1}{2\,\Pi} \sum_{i=1}^{n} \frac{1}{C_i R_i}$$

Page 710, line 2

$$f_L = \frac{\omega_L}{2_\Pi} = \frac{1}{2\Pi}\left[\frac{1}{C_{C1}R_{C1}} + \frac{1}{C_E R_{CE}} + \frac{1}{C_{C2}R_{C2}}\right]$$

Page 710, line 13

… may select C_E so that $1/(C_E R_{CE})$ is, say…

Page 718, line 4

$$C_\mu = \frac{C_{\mu 0}}{\left(1+\frac{V_{CB}}{V_{0c}}\right)^m}$$

Page 760, Exercise 10.22, last line

…C_L must be reduced to 1.41 pF.

Page 763, line 8

$$\frac{V_O}{V_{\text{sig}}}(s) = A_M \frac{1+\left(\frac{s}{\omega_z}\right)}{1+ b_1 s + b_s s^2}$$

Page 788, right-hand column, line 24

… $f_H = (1/2\pi R'_{\text{sig}} C_{\text{in.}})$

Page 799, right-hand column, 10th line from bottom

…show that the pole introduced at the output node is dominant.

Page 834, Example 11.4, sixth line from bottom

$$A \equiv \frac{V_o}{V_i} = \mu \frac{R_L \| (R_1 + R_2)}{[R_L \| (R_1 + R_2)] + r_o} \frac{R_{id}}{R_{id} + R_s + (R_1 \| R_2)}$$

Page 839, Exercise 11.8, last line

Ans. 0.5 mA, 0.5 mA, 5 mA, 85 V/V; 0.1 V/V; 8.95 V/V; 189.5 kΩ; 19.2 Ω.

Page 855, Exercise 11.17, second-to-last line

Ans. $A\beta = 249.3$ …

Page 863, line 8

$$R_{in} = \frac{1}{\frac{1}{R_{if}} - \frac{1}{R_s}} - \frac{1}{\frac{1}{1.11} - \frac{1}{1000}} \cong 1.11\ \Omega$$

Page 884, Exercise 11.25

Figure is E11.25.

Page 948, Exercise 12.10, third-to-last line

(b) For $\beta_P = 200, \beta_N = 50, I_{SP} = 10^{-14}$A, …

Page 969

Figure correction: see end of document.

Page 989, left-hand column, line 25

$$\frac{v_o}{v_i} = \frac{R_L}{R_L + (1/2g_m)}$$

Page 992, left-hand column, Line 18

…η and evaluate the value of η for the case $f_s = 250$ kHz, R=16Ω, …

Page 1011, line 6

... provides a bias line for Q_5 and Q_7 of the CMOS op-amp circuit of Fig. 13.1.

Page 1011, line 22

… in which we recognize the factor $\sqrt{2\mu_n C_{ox}(W/L)_{12} I_{REF}}$ as g_{m12}; thus,…

Page 1015, line 3

The PSRR is determined using Eq. (13.54):

Page 1017

Figure correction: see end of document.

Page 1034, Exercise 13.18, line 2

…all three transistors is 10^{-14} A. Find V_{BE6}, V_{R3}, and I_{C7}.

Page 1036, Example 13.3, line 4

Reference to Fig 13.17 shows that…

Page 1040, Exercise 13.23, line 3

Ans. 2.63 kΩ; 0.38 mA/V; 0.19 mA/V; 2.1 MΩ

Page 1046, Exercise 13.32, third-to-last line

Ans. 90.9 kΩ; 722 kΩ; 81 kΩ

Page 1080, right-hand column, ninth line from bottom

… these values with the original ones, namely $R_{id} = 2.1$ MΩ, …

Page 1081, right-hand column, line 14

... at 19μA.

Page 1087, line 24

…knowledge of the MOSFET internal capacities (Section 10.2.1) will be needed.

Page 1098, line 4

…in Section 15.4, we shall…

Page 1100, line 9

Refer to the inverter shown in block form in Fig. 14.2(a). …

Page 1112

Figure correction: see end of document.

Page 1128, Exercise 14.9, line 1

For the inverter of Fig 14.18(a), let the on-resistance of PU be 20 kΩ and that of $PD = 10$ kΩ….

Page 1131, line 14

$$t_{PLH} = \frac{\alpha_{pC}}{k'_p(W/L)_p V_{DD}}$$

Page 1133, seventh line from bottom

$$t_{PLH} \cong R_P C$$

Page 1137, ninth line from bottom

...given in Eq. (10.25) for calculating C_{db1} and C_{db2} is a small-signal relationship, ...

Page 1150, starting with 10th line from bottom

This energy is dissipated in the on-resistance of switch PD and is converted to heat.

Next consider the situation when v_I goes high. The pull-up switch PD turns off and the pull-down switch P turns on.

Page 1150, Second line from bottom

This amount of energy is dissipated in the on-resistance of switch PD and is converted to heat.

Page 1153

Delete line 23.

Page 1158

Figure correction: please see end of document.

Page 1160, right-hand column, line 9

…on-resistance of PU be 2 kΩ and that of PD be 1 kΩ.

Page 1161, line 17

…As will be seen in Section 15.1.3, …

Page 1197, line 19

We can now compute the average charging current as…

Page 1215, exercise 15.15, line 9

…technology has the parameter values specified in Example 15.3 and that for all NMOS transistors in…

Page 1229, left-hand column, line 22

0.4 V, and $V_{DD} = 1.3$ V, find V_{OH}, V_{OL}, and $I_{stat.}$

Page 1232, line 12

…on, is approximately $V_{DD}/2$ and thus occurs at $t \cong t_{PLH}$.

Page 1269

Figure correction: see end of document.

Page 1281, last line

…transistor Q_P resets the internal node…

Page 1370

Figure correction: see end of document.

Page 1398

Figure correction: see end of document.

Page 1400, Exercise 18.10, second line

…Eq. (18.17) and that for oscillations to start $g_m R > (L_1/L_2)$ where R is the total resistance between collector and emitter.

Page 1430, right-hand column, second line from bottom

D 18.20 For the circuit in Fig. P18.20,…

Appendices on Companion Website Page

Line 10

Part B.1 describes the models SPICE programs use…

Line 12

Part B.2 describes and discusses…

Line 13

…while part B.3 does…

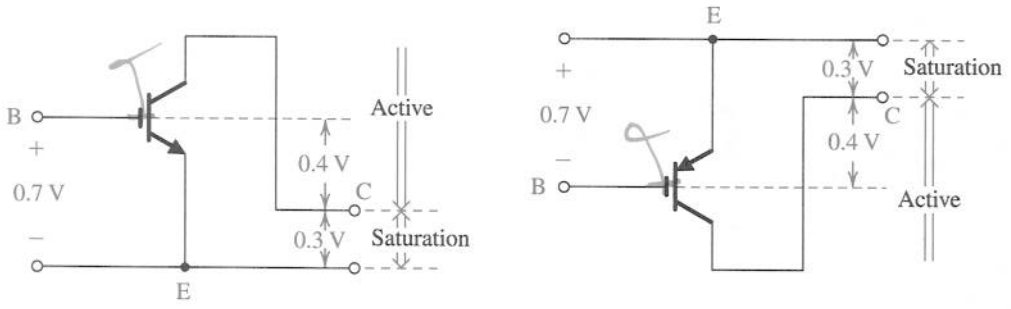
Line 17

…This appendix summarizes the *y*, …

Line 26

Appendix F: *s*-Domain Analysis: Poles, Zeros, and Bode Plots

The following pages contain corrections to figures.



(a) *npn* (b) *pnp*

Figure 6.14 Graphical representation of the conditions for operating the BJT in the active mode and in the saturation mode.

Table 6.2 Summary of the BJT Current–Voltage Relationships in the Active Mode

$$i_C = I_S e^{v_{BE}/V_T}$$

$$i_B = \frac{i_C}{\beta} = \left(\frac{I_S}{\beta}\right) e^{v_{BE}/V_T}$$

$$i_E = \frac{i_C}{\alpha} = \left(\frac{I_S}{\alpha}\right) e^{v_{BE}/V_T}$$

Note: For the *pnp* transistor, replace v_{BE} with v_{EB}.

$$i_C = \alpha i_E \qquad i_B = (1-\alpha) i_E = \frac{i_E}{\beta+1}$$

$$i_C = \beta i_B \qquad i_E = (\beta+1) i_B$$

$$\beta = \frac{\alpha}{1-\alpha} \qquad \alpha = \frac{\beta}{\beta+1}$$

V_T = thermal voltage = $\frac{kT}{q} \simeq 25$ mV at room temperature

For greater emphasis, we show in Fig. 6.14 a graphical construction that illustrates the conditions for operating the BJT in the active mode and in the saturation mode. Also, for easy reference, we present in Table 6.2 a summary of the BJT current–voltage relationships in the active mode of operation.

The Collector–Base Reverse Current (I_{CBO}) In our discussion of current flow in transistors we ignored the small reverse currents carried by thermally generated minority carriers. Although such currents can be safely neglected in modern transistors, the reverse current across the collector–base junction deserves some mention. This current, denoted I_{CBO}, is the reverse current flowing from collector to base with the emitter open-circuited (hence the subscript O). This current is usually in the nanoampere range, a value that is many times higher than its theoretically predicted value. As with the diode reverse current, I_{CBO} contains a substantial leakage component, and its value is dependent on v_{CB}. I_{CBO} depends strongly on temperature, approximately doubling for every 10°C rise.[6]

[6] The temperature coefficient of I_{CBO} is different from that of I_S because I_{CBO} contains a substantial leakage component.

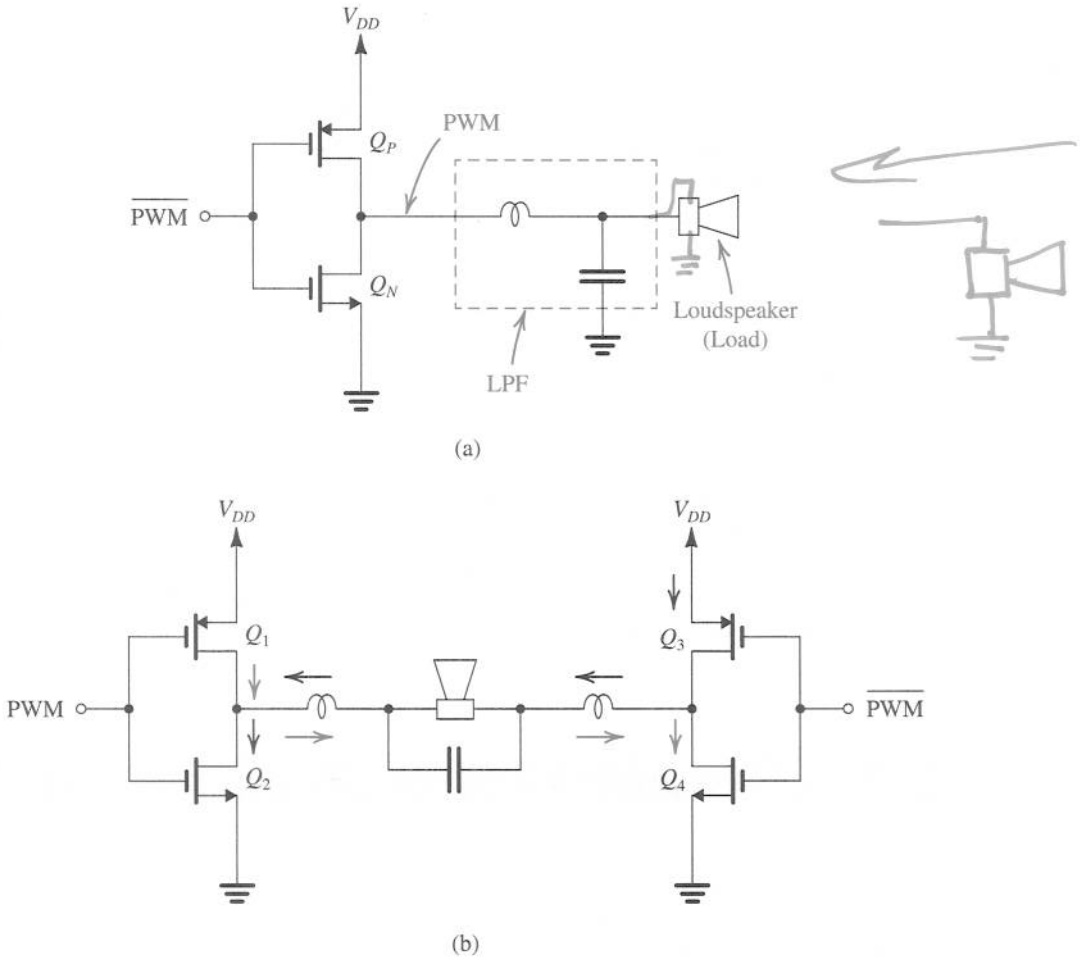


Figure 12.34 Two schemes for driving the load of a class D amplifier. The differential scheme in (**b**) results in doubling the voltage excursion across the load.

Having obtained a pulse waveform in which the audio signal is encoded, we now show how the PWM signal can be used to drive the switches that supply the load power. Two alternative schemes for accomplishing this task are shown in Fig. 12.34. In Fig. 12.34(a), the logical inverse of PWM, denoted $\overline{\text{PWM}}$ and obtained from the comparator by simply exchanging the terminals to which v_A and v_T are applied, is used to drive two complementary MOS switches Q_P and Q_N. These switches connect the output node alternatively to V_{DD} and ground, in effect producing a high-power version of PWM at their drain node. This is the signal applied to the load (shown as a loudspeaker) through a low-pass filter. It follows that v_A appears across the load and the large current required by the low-resistance load is supplied by Q_P and Q_N.

To double the voltage excursion across the load, the scheme in Fig. 12.34(b) can be utilized. Here both PWM and its logical inverse $\overline{\text{PWM}}$ are used in a differential driving arrangement. When PWM is high and thus $\overline{\text{PWM}}$ is low, Q_3 and Q_2 are turned on while Q_1 and Q_4 are off. Thus current flows from V_{DD} to ground through the load (from right to left). The opposite happens when PWM is low. Thus the voltage across the load will be twice that obtained with

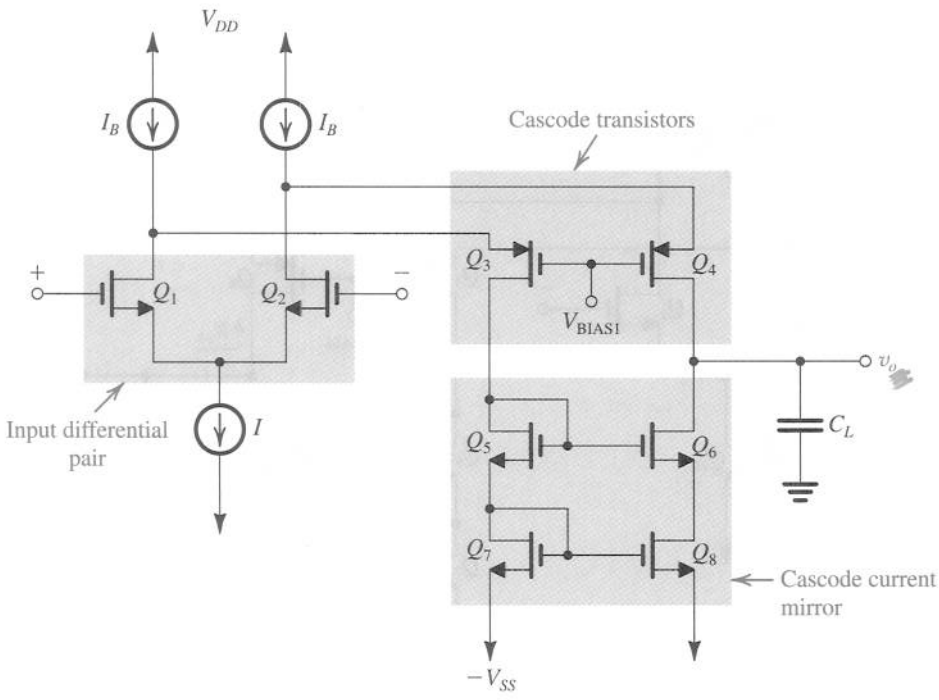


Figure 13.9 Structure of the folded-cascode CMOS op amp.

EXERCISE

13.9 To limit the power dissipation in the op-amp circuit of Fig. 13.9 to an acceptable level, the total dc current is limited to 0.3 mA. If it is desired to bias each of Q_1 and Q_2 at a dc current four times the bias current of each of Q_3 and Q_4, find the values of I_B, I, $I_{D1,2}$, and $I_{D3,4}$.
Ans. 150 μA; 240 μA; 120 μA; 30 μA

As we learned in Chapter 8, if the full advantage of the high output resistance achieved through cascoding is to be realized, the output resistance of the current-source load must be equally high. This is the reason for using the cascode current mirror Q_5 to Q_8 in the circuit of Fig. 13.9. (This current-mirror circuit was studied in Section 8.6.1.) Finally, note that capacitance C_L denotes the total capacitance at the output node. It includes the internal transistor capacitances, an actual load capacitance (if any), and possibly an additional capacitance deliberately introduced for the purpose of frequency compensation. In many cases, however, the load capacitance will be sufficiently large, obviating the need to provide additional capacitance to achieve the desired frequency compensation. This topic will be discussed shortly. For the time being, we note that unlike the two-stage circuit, which requires

EXERCISES

D14.3 In an attempt to reduce the required value of R_D to 10 kΩ, the designer of the inverter in Example 14.2 decides to keep the parameter V_x unchanged but increases W/L. What is the new value required for W/L? Do the noise margins change? What does the power dissipation become?
Ans. 3.75; no; 151 μW

D14.4 In an attempt to reduce the required value of R_D to 10 kΩ, the designer of the inverter in Example 14.2 decides to change V_x while keeping W/L unchanged. What new value of V_x is needed? What do the noise margins become? What does the power dissipation become?
Ans. $V_x = 0.22$ V; $NM_L = 0.46$ V, $NM_H = 0.49$ V; 139 μW

Example 14.3 The Pseudo-NMOS Inverter

To eliminate the problem associated with the need for a large resistance R_D in the circuit of Fig. 14.20(a), studied in Example 14.2, R_D can be replaced by a MOSFET. One such possibility is the circuit in Fig. 14.21, where the load is a PMOS transistor Q_P whose gate is tied to ground in order to turn it on. Because of its resemblance to an earlier form of logic (NMOS logic, now obsolete) in which the load is an NMOS transistor, this circuit is known as a pseudo-NMOS inverter.

(a) Assuming $\lambda_1 = \lambda_2 = 0$, $V_{tn} = -V_{tp} = V_t$, and $k_n = 5k_p$, find V_{OH} and V_{OL}.
(b) For $k_n = 300$ μA/V^2, $V_t = 0.4$ V, and $V_{DD} = 1.8$ V, evaluate the values of V_{OH} and V_{OL} and find the average power dissipated in the inverter, assuming it spends half the time in each of its two states.

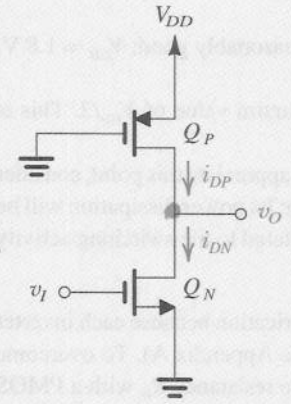


Figure 14.21 Pseudo-NMOS inverter for Example 14.3.

(c) Find the power dissipation in the inverter in the two cases: (i) the output is low, and (ii) the output is high and driving the maximum fan-out found in (b).

14.21 For an inverter employing a 2-V supply, suggest an ideal set of values for V_M, V_{IL}, V_{IH}, V_{OL}, V_{OH}, NM_L, NM_H. Also, sketch the VTC. What value of voltage gain in the transition region does your ideal specification imply?

14.22 For a particular inverter, the basic technology used provides an inherent limit to the small-signal, low-frequency voltage gain of 50 V/V. If, with a 2-V supply, the values of V_{OL} and V_{OH} are ideal, but $V_M = 0.4V_{DD}$, what are the best possible values of V_{IL} and V_{IH} that can be expected? What are the best possible noise margins you could expect? Find the large-signal voltage gain, where the gain is defined by $(V_{OH} - V_{OL})/(V_{IL} - V_{IH})$. (*Hint:* Use straight-line approximations for the VTC.)

***14.23** A logic-circuit type intended for use in a digital-signal-processing application in a newly developed hearing aid can operate down to single-cell supply voltages of 1.2 V. If for its inverter, the output signals swing between 0 and V_{DD}, the "gain-of-one" points are separated by less than $\frac{1}{3}$ V_{DD}, and the noise margins are within 30% of one another, what ranges of values of V_{IL}, V_{IH}, V_{OL}, V_{OH}, NM_L, and NM_H can you expect for the lowest possible battery supply?

D 14.24 Design the inverter circuit in Fig. 14.12(a) to provide $V_{OH} = 1.2$ V, $V_{OL} = 50$ mV, and so that the current drawn from the supply in the low-output state is 30 μA. The transistor has $V_t = 0.4$ V, $\mu_n C_{ox} = 500$ μA/V^2, and $\lambda = 0$. Specify the required values of V_{DD}, R_D, and W/L. How much power is drawn from the supply when the output is high? When the output is low?

14.25 For the current-steering circuit in Fig. 14.19, $V_{CC} = 2$ V, $I_{EE} = 0.5$ mA, find the values of R_{C1} and R_{C2} to obtain a voltage swing of 0.5 V at each output. What are the values realized for V_{OH} and V_{OL}?

D 14.26 Refer to the analysis of the resistive-load MOS inverter in Example 14.2 and utilize the expressions derived there for the various inverter parameters. Design the circuit to satisfy the following requirements: $V_{OH} = 1.2$ V, $V_{OL} = 50$ mV, and the power dissipation in the low-output state = 60 μW. The transistor available has $V_t = 0.4$ V, $\mu_n C_{ox} = 500$ μA/V^2, and $\lambda = 0$. Specify the required values of V_{DD}, R_D, and W/L. What are the values obtained for V_{IL}, V_M, V_{IH}, NM_L, and NM_H?

D 14.27 Refer to the analysis of the resistive-load MOS inverter in Example 14.2 and utilize the expressions derived there for the various inverter parameters. For a technology for which $V_t = 0.3V_{DD}$, it is required to design the inverter to obtain $V_M = V_{DD}/2$. In terms of V_{DD}, what is the required value of the design parameter V_x? What values are obtained for V_{OH}, V_{OL}, V_{IL}, V_{IH}, NM_H, and NM_L, in terms of V_{DD}? Give numerical values for the case $V_{DD} = 1.2$ V. Now, express the power dissipated in the inverter in its low-output state in terms of the transistor's W/L ratio. Let $k_n' = 500$ μA/V^2. If the power dissipation is to be limited to approximately 100 μW, what W/L ratio is needed and what value of R_D corresponds?

14.28 An earlier form of logic circuits, now obsolete, utilized NMOS transistors only and was appropriately called NMOS logic. The basic inverter, shown in Fig. P14.28, utilizes an NMOS driver transistor Q_1 and another NMOS transistor Q_2, connected as a diode, forms the load of the inverter. Observe that Q_2 operates in saturation at all times. Assume $V_{t1} = V_{t2} = V_t$, $\lambda_1 = \lambda_2 = 0$, and denote $\sqrt{k_{n1}/k_{n2}}$ by k_r. Also neglect the body effect in Q_2 (note that the body of Q_2, not shown, is connected to ground).

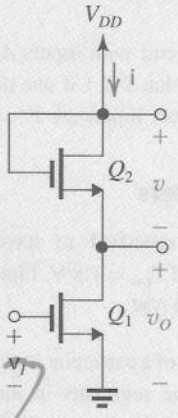


Figure P14.28

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

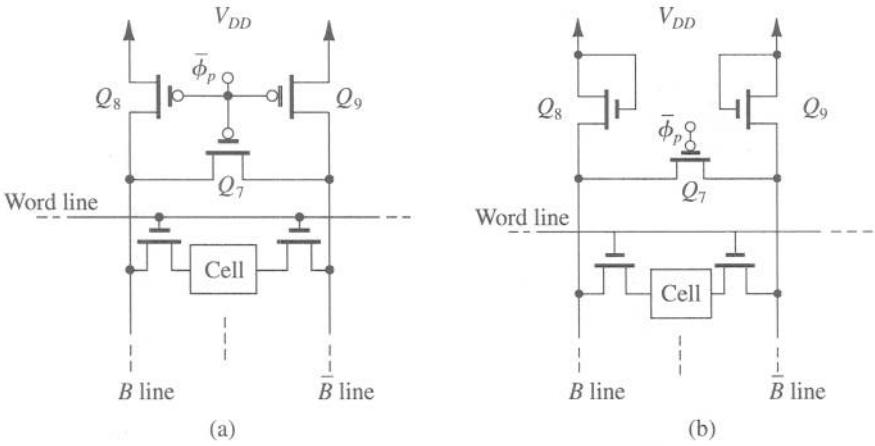


Figure 16.23 Two alternative arrangements for precharging the bit lines: (**a**) The B and $\overline{B}$ lines are precharged to V_{DD}; (**b**) the B and $\overline{B}$ lines are charged to $(V_{DD} - V_t)$.

the small difference signals that appear between B and $\overline{B}$ as a result of the read operation of a cell connected to the B and $\overline{B}$ lines.

The amplifier is designed so that in normal small-signal operation, all transistors operate in the saturation region. Figure 16.24(b) shows the amplifier in its equilibrium state with $v_B = v_{\overline{B}} = V_{DD} - V_t$. Note that we have assumed that the B and $\overline{B}$ lines are precharged to $(V_{DD} - V_t)$ using the circuit in Fig. 16.23(b). It turns out that this voltage is particularly convenient for the operation of this amplifier type as a sense amplifier. As indicated in Fig. 16.24(b), the bias current I divides equally between Q_1 and Q_2; thus each conducts a current $I/2$. The current of Q_1 is fed to the input side of the current mirror, transistor Q_3; thus the mirror provides an equal output current $I/2$ in the drain of Q_4. At the output node, we see that we have two equal and opposite currents, leaving a zero current to flow into the load capacitor. Thus, in an ideal situation of perfect matching, v_O will be equal to the voltage at the drain of Q_1.

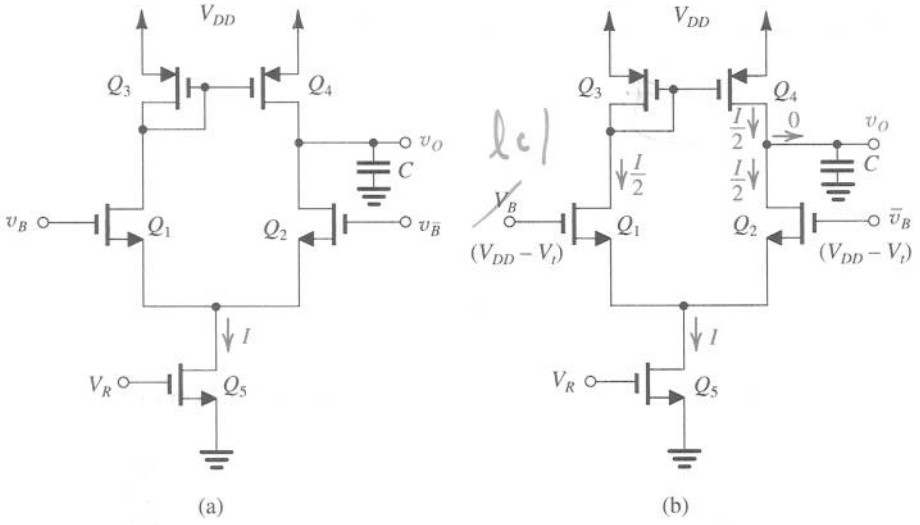


Figure 16.24 The currrent-mirror-loaded MOS differential amplifier as a sense amplifier.

***17.3** A filter has the transfer function $T(s) = 1/[(s+1)(s^2+s+1)]$. Show that $|T| = \sqrt{1+\omega^6}$ and find an expression for its phase response $\phi(\omega)$. Calculate the values of $|T|$ and ϕ for $\omega = 0.1$, 1, and 10 rad/s and then find the output corresponding to each of the following input signals:

(a) 10 sin 0.1t (volts)
(b) 10 sin t (volts)
(c) 10 sin 10t (volts)

17.4 For the filter whose magnitude response is sketched (as the blue curve) in Fig. 17.3, find $|T|$ at $\omega = 0$, $\omega = \omega_p$, and $\omega = \omega_s$. $A_{max} = 0.2$ dB, and $A_{min} = 60$ dB.

D 17.5 A low-pass filter is required to pass all signals within its passband, extending from 0 to 4 kHz, with a transmission variation of at most 5% (i.e., the ratio of the maximum to minimum transmission in the passband should not exceed 1.05). The transmission in the stopband, which extends from 5 kHz to ∞, should not exceed 0.05% of the maximum passband transmission. What are the values of A_{max}, A_{min}, and the selectivity factor for this filter?

17.6 A low-pass filter is specified to have $f_p = 5$ kHz and a selectivity factor of 10. The specifications are just met by a first-order transfer function

$$T(s) = \frac{2\pi \times 10^4}{s + 2\pi \times 10^4}$$

What must A_{max} and A_{min} be?

17.7 A low-pass filter is specified to have $A_{max} = 2$ dB and $A_{min} = 12$ dB. It is found that these specifications can be just met with a single-time-constant RC circuit having a time constant of 1 s and a dc transmission of unity. What must ω_p and ω_s of this filter be? What is the selectivity factor?

17.8 Sketch transmission specifications for a high-pass filter having a passband defined by $f \geq 3$ kHz and a stopband defined by $f \leq 2$ kHz. $A_{max} = 0.4$ dB, and $A_{min} = 60$ dB.

17.9 Sketch transmission specifications for a bandstop filter that is required to pass signals over the bands $0 \leq f \leq 10$ kHz and 20 kHz $\leq f \leq \infty$ with A_{max} of 0.5 dB. The stopband extends from $f = 12$ kHz to $f = 18$ kHz, with a minimum required attenuation of 50 dB.

Section 17.2: The Filter Transfer Function

17.10 Consider a fifth-order filter whose poles are all at a radial distance from the origin of 10^4 rad/s. One pair of complex-conjugate poles is at 18° angles from the $j\omega$ axis, and the other pair is at 54° angles. Give the transfer function in each of the following cases.

(a) The transmission zeros are all at $s = \infty$ and the dc gain is unity.
(b) The transmission zeros are all at $s = 0$ and the high-frequency gain is unity.

What type of filter results in each case?

17.11 A third-order low-pass filter has transmission zeros at $\omega = 2$ rad/s and $\omega = \infty$. Its natural modes are at $s = -1$ and $s = -0.5 \pm j0.8$. The dc gain is unity. Find $T(s)$.

17.12 A second-order low-pass filter has poles at $-0.25 \pm j$ and a transmission zero at $\omega = 2$ rad/s. If the dc gain is unity, give the transfer function $T(s)$. What is the gain at ω approaching infinity?

17.13 Find the order N and the form of $T(s)$ of a bandpass filter having transmission zeros as follows: one at $\omega = 0$, one at $\omega = 10^3$ rad/s, one at 3×10^3 rad/s, one at 6×10^3 rad/s, and one at $\omega = \infty$. If this filter has a monotonically decreasing passband transmission with a peak at the center frequency of 2×10^3 rad/s, and equiripple response in the stopbands, sketch the shape of its $|T|$.

***17.14** Analyze the RLC network of Fig. P17.14 to determine its transfer function $V_o(s)/V_i(s)$ and hence its poles and zeros. (*Hint:* Begin the analysis at the output and work your way back to the input.)

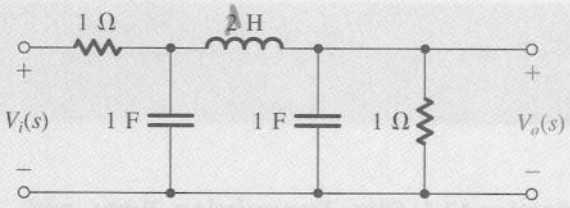


Figure P17.14

Section 17.3: Butterworth and Chebyshev Filters

D 17.15 Determine the order N of the Butterworth filter for which $A_{max} = 0.5$ dB, $A_{min} \geq 20$ dB, and the selectivity ratio $\omega_s/\omega_p = 1.7$. What is the actual value of minimum stopband attenuation realized? If A_{min} is to be exactly 20 dB, to what value can A_{max} be reduced?

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

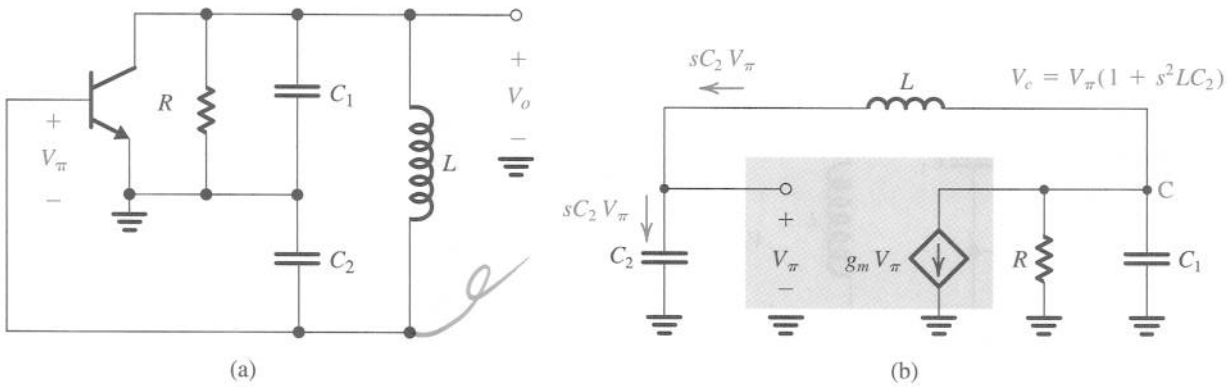


Figure 18.14 (**a**) A Colpitts oscillator in which the emitter is grounded and the output is taken at the collector. (**b**) Equivalent circuit of the Colpitts oscillator of (**a**). To simplify the analysis, C_μ and r_π are neglected. We can consider C_π to be part of C_2, and we can include r_o in R.

Using the alternative analysis approach described in Section 18.1.3, we analyze the circuit as shown in Fig. 18.14(b). A node equation at the transistor collector (node C) yields

$$sC_2V_\pi + g_mV_\pi + \left(\frac{1}{R} + sC_1\right)(1 + s^2LC_2)V_\pi = 0$$

Since $V_\pi \neq 0$ (oscillations have started), it can be eliminated, and the equation can be rearranged in the form

$$s^3LC_1C_2 + s^2(LC_2/R) + s(C_1 + C_2) + \left(g_m + \frac{1}{R}\right) = 0 \tag{18.18}$$

Substituting $s = j\omega$ gives

$$\left(g_m + \frac{1}{R} - \frac{\omega^2LC_2}{R}\right) + j\left[\omega(C_1 + C_2) - \omega^3LC_1C_2\right] = 0 \tag{18.19}$$

For oscillations to start, both the real and imaginary parts must be zero. Equating the imaginary part to zero gives the frequency of oscillation as

$$\omega_0 = 1\Big/\sqrt{L\left(\frac{C_1C_2}{C_1 + C_2}\right)} \tag{18.20}$$

which is the resonance frequency of the tank circuit, as anticipated.[3] Equating the real part to zero and using Eq. (18.20) gives

$$C_2/C_1 = g_mR \tag{18.21}$$

which has a simple physical interpretation: For sustained oscillations, the magnitude of the gain from base to collector (g_mR) must be equal to the inverse of the voltage ratio provided by the capacitive divider, which from Fig. 18.14(a) can be seen to be $V_{eb}/V_{ce} = C_1/C_2$. Of course, for oscillations to start, the loop gain must be made greater than unity, a condition that can be

[3] If r_π is taken into account, the frequency of oscillation can be shown to shift slightly from the value given by Eq. (18.20).