ECE 342 Fall 2017 Optoelectronic Link Project

Lab3: MOSFET Based Logic Gates and the Digital Oscillator

Overview

This lab investigates the use of metal-oxide-semiconductor field effect transistors (MOSFETs) to implement logic gates, with the aim of developing the clock circuit for the transmitter. For a detailed discussion of MOSFET logic circuits, refer to Chapter 14 of your textbook. The clock circuit will be implemented as a digital oscillator based on the ring oscillator

Inverter Characteristics

Figure 1 shows the prototypical voltage transfer characteristic (VTC) of a logic inverter, illustrating the definition of the critical points of an inverter. The red line in the figure is the ideal inverter VTC. The definitions of the critical points and noise margins are given in Table 1. These concepts should be familiar from ECE 275, even if the reasons for their existence are topics of ECE 342, 343 and 445.

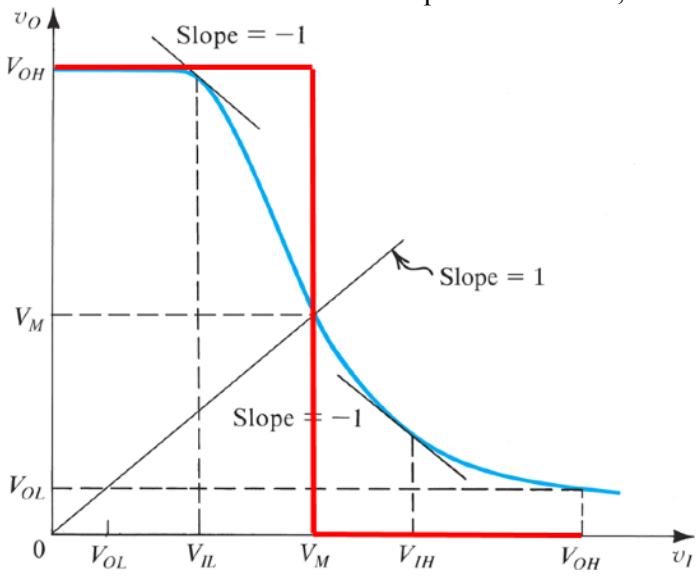

Figure 1. Typical VTC of a logic inverter (figure from [1]).

Table 1. Important parameters of the VTC of the logic inverter

V_{OL}	output low level
V_{OH}	output high level
V_{IL}	maximum value of the input interpreted by the inverter as a logic 0
V_{IH}	minimum value of the input interpreted by the inverter as a logic 1
NM_L	noise margin for low input = V_{IL}-V_{OL}
NM_H	noise margin for high input = V_{OH} - V_{IH}

Figure 2 shows how rise and fall times are defined for a logic signal. The rise time t_r is defined as the length of time the signal goes from 10% to 90% of the V_{OL} to V_{OH} transition, while fall time t_f is defined as the length of time the signal goes from 90% to 10% of the V_{OH} to V_{OL} transition.

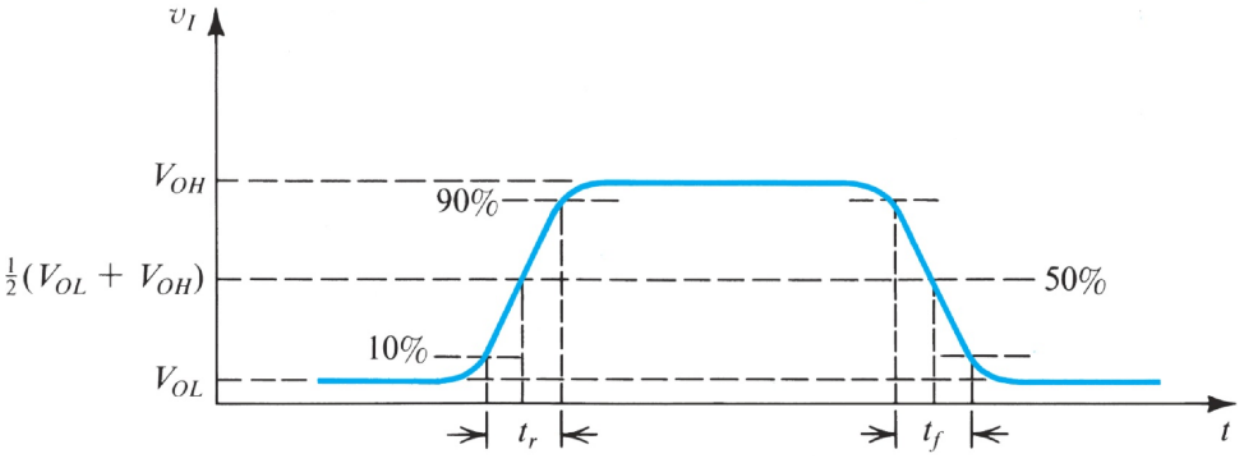

Figure 2. Definition of rise and fall times (figure from [1])

NMOS Inverter

The basic resistively loaded n-type MOSFET (***NMOS***) common-source inverting amplifier circuit (figure 3a) can be used as a logic inverter, as can be seen from its voltage transfer characteristic (VTC) (figure 3b). The origins of the parameters defined in table 1 and figure 1 can be deduced from the VTC of this circuit. The load of an NMOS logic gate will most likely be another such logic gate, which will correspond to the gate terminal of its MOSFET, Q_2. Hence, the load can be treated as purely capacitive. The maximum output voltage V_{OH} will be V_{DD}, as no current will flow through R_D when Q_1 is off. However, V_{OL} will not be the ideal 0V, as Q_1 and R_D will reach a balance so that Q_1 will be in triode mode. In this part of the experiment, DC and AC characteristics of the NMOS inverter, including power consumption and switching speed will be investigated.

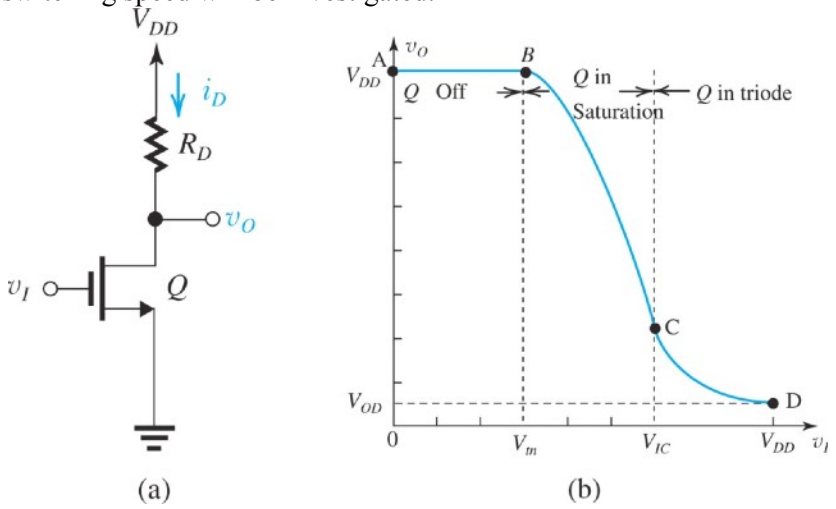

Figure 3. (a) Resistively loaded NMOS CS inverting amplifier and **(b)** its voltage transfer characteristic. (figure from [1])

CMOS Inverter

The complementary MOSFET (***CMOS***) (figure 4) has superior DC and AC characteristics compared to most other logic families. In particular, the CMOS circuit has a rail-to-rail output voltage swing, and zero DC power consumption. DC and AC characteristics of the CMOS inverter, including power consumption and switching speed will be investigated

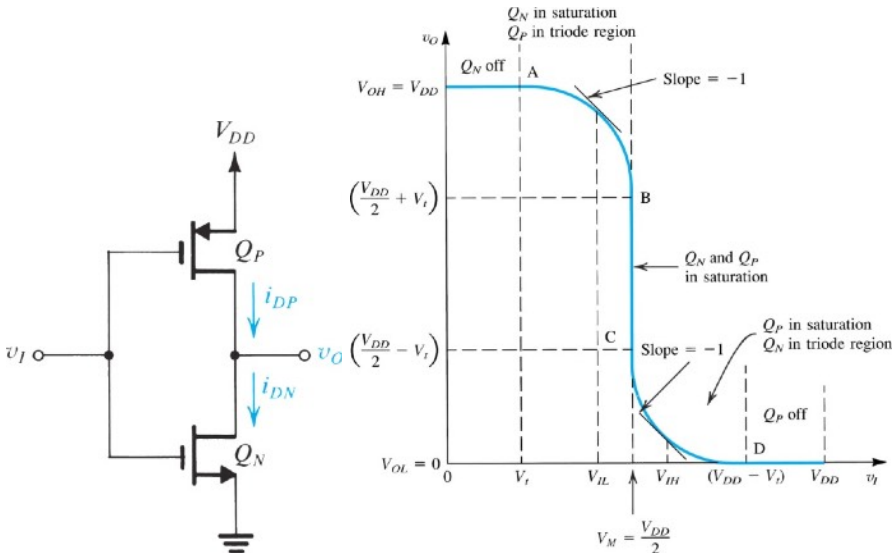

Figure 4. (a) CMOS inverter and **(b)** its voltage transfer characteristic (figure from [1]).

The Ring Oscillator (Section 16.4.4)

The ring oscillator, whose basic topology is shown in figure 5, is a digital oscillator circuit that is commonly used for on-chip clock generation, as well as demonstrating the speed limits of an IC fabrication technology. An *odd* number of inverters are connected in series, with the output of the last inverter fed back to the input of the first inverter. If the output of the first inverter is high (i.e. its input low), the output of the last inverter will also go high, thus pulling the input of the first inverter high. This will flip the output of the first inverter to low, resulting in the output of the last inverter going low, flipping the output of the first inverter high again. Due to the finite propagation delay through each gate, the inverter will oscillate at a finite frequency given by $f_{osc} = \frac{1}{2n\tau_p}$, where n is the number of inverters in the chain, and τ_p is the propagation delay of an individual inverter. Note that an even number of inverters would have resulted in a stable output.

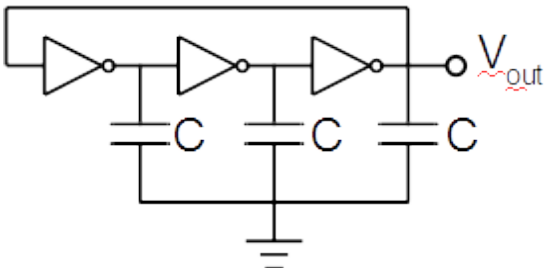

Figure 5. Ring oscillator for clock signal generation.

Ring oscillators are commonly used to demonstrate the high frequency performance of integrated circuits. A typical ring oscillator may have between 127 and 255 inverters. The desired clock signal is 20 kHz, and the internal capacitances of the CD4007 MOSFETs are too small for oscillation in the kHz range. Therefore, external capacitors would be required to load each node as shown in Figure 5 to increase the propagation delay. Even though Figure 5 implies the three capacitors need to be equal, different valued capacitors can be used to fine tune the circuit.

In this lab, you will design a three-stage CMOS ring oscillator using the MOSFETs on the CD4007 chip. The ring oscillator should oscillate at 20 kHz with a ±5% tolerance. In your simulations, you will use the CD4007 SPICE model developed by Dr. Fuller at RIT. The model is not perfect and you may need to

modify the capacitor values to obtain a clock frequency of 20 kHz with a ±5% tolerance. You will also see a rounded, almost sinusoidal, output signal, instead of a flat-top square wave with 50% duty cycle. This is because three inverters are too few to implement a digital, i.e. square-wave, oscillator. On-chip ring oscillators may use 127 or even 255 inverters! We will design and implement a circuit in Lab 4 to take this imperfect clock signal and generate a 50% duty cycle square wave to drive the LED of the transmitter.

The Astable Multivibrator

An alternative clock generator circuit is the astable multivibrator, shown in figure 6 below. The period is set by choosing appropriate values for R and C. This circuit has several advantages over the ring oscillator: (i) the output is nearly a perfect square wave; (ii) the duty cycle is close to 50%; (iii) it requires only two components, one of which is a resistor.

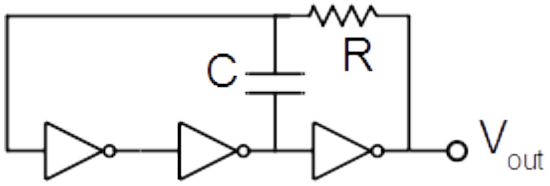

Figure 6. Ring oscillator for clock signal generation.

In this task, you will design an astable multivibrator using the MOSFETs on the CD4007 chip. The circuit should oscillate at 20 kHz, within the specified ±5% tolerance.

Two Input Logic Gates

Finally, two input CMOS gates will be studied. Figure 7(a) shows a two input CMOS NOR gate while figure 7(b) shows a two input NAND gate. Odd numbered teams will construct and test NAND and AND gates, while even numbered teams will construct and test NOR and OR gates using the CD4007 integrated circuit which contains three NMOS-PMOS pairs.

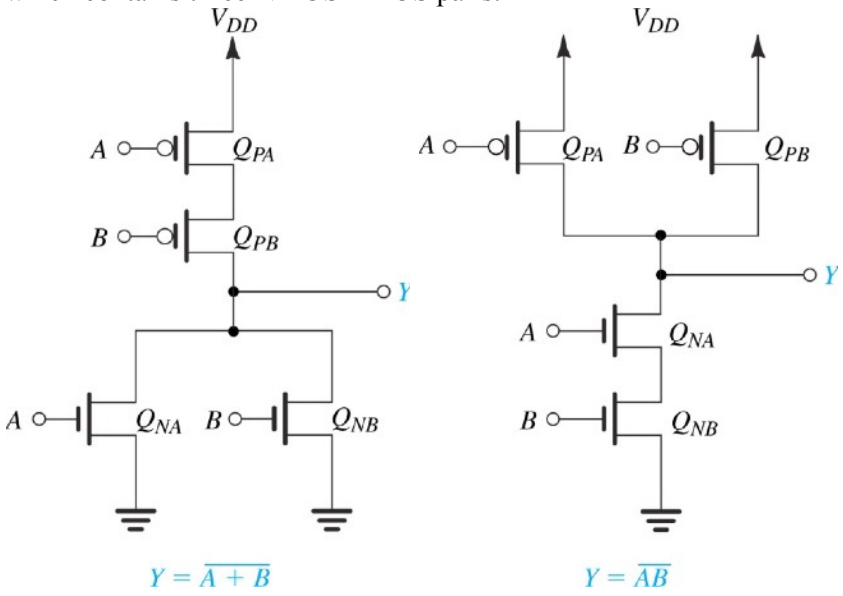

Figure 7. (a) Two input NOR gate and **(b)** two input NAND gate (figure from [1]).

The CD4007

The data sheet for the CD4007UBE is available on the course web page. The connection diagram is replicated in Figure 8. The CD4007 has three NMOS and three PMOS transistors, connected in three pairs. The first two pairs (N1-P1 and N2-P2) have their gates connected together, while the third pair (N3-P3) have both their gates and drains connected together. Hence, the third pair is ideal for implementing a single inverter. All PMOS substrate terminals are connected to V_{DD} and all NMOS substrate terminals are connected to VSS. In the experiments, V_{SS} will be connected to ground, and V_{DD} to the positive supply voltage (+5V in most cases).

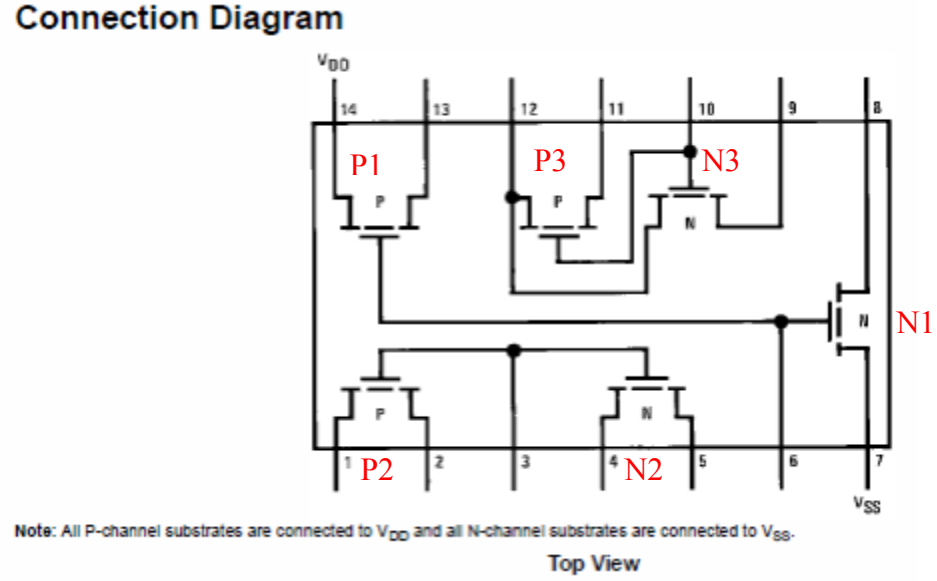

Figure 8. Pin connection diagram of the CD4007C (figure from [2]).

Tasks

1. ***NMOS Inverter Design and Simulation:*** Design an NMOS inverter based on the CD4007 NMOS. ***(i)*** Calculate the value of the resistor R_D required to set V_{out} = 2.5V when V_{in} = 2.5V. ***(ii)*** Simulate V_{OL} vs. R_D, by varying R_D from 1 kΩ to 100 kΩ. ***(iii)*** Plot the voltage transfer characteristic of this logic inverter gate for R_D = 1 kΩ, 100 kΩ and the value you calculated. Determine the DC power consumed by the gate when $V_{out} = V_{OH}$ and $V_{out} = V_{OL}$ for these values of R_D, assuming it is driving a second identical inverter. ***(iv)*** Simulate the transient characteristics of the inverter assuming it is driving a second identical inverter, for the same three values of R_D. You can model the parasitic capacitance of your prototyping board with a 10 pF capacitance at the output of each inverter. Determine the rise and fall time for each R_D value. Which component determines which time constant? Is there a trade-off among DC power consumption, V_{OL} and t_{rise} and/or t_{fall}? Do another transient simulation, for V_{DD} = +10V and V_{DD} = +15V for the resistor value you calculated. Do the rise and fall times depend on the supply voltage?
2. ***CMOS Inverter Design and Simulation:*** Design a circuit in which three CMOS inverters are connected in series using the CD4007 MOSFETs. Model the breadboard's parasitic capacitances by loading each node with a 10 pF capacitor. ***(i)*** Simulate the circuit and plot the VTC of the first stage. ***(ii)*** Determine the rise and fall times of the first stage when it is loaded with another CMOS gate as described. ***(iii)*** Determine the propagation delay of the gates by comparing the delay from the input to the output of the second stage.
3. ***CMOS Ring Oscillator Design and Simulation:*** Design a ring oscillator circuit in which three CMOS inverters are connected in series using the CD4007, with the output of the last inverter connected to the input of the first inverter and a capacitor C is connected to each output. Determine the value of

this capacitor C which will result in an oscillation at your assigned frequency. What is the duty cycle of the output signal? Perform a sensitivity analysis to predict the expected variation in oscillation frequency due to a 5% and 10% capacitor tolerance.

4. ***Astable Multivibrator Design and Simulation:*** Design an astable multivibrator using the CD4007. Determine the value of the capacitor C and resistor R which will result in an oscillation at your assigned frequency. What is the duty cycle of the output signal?

5. ***NMOS Inverter Construction and Testing:*** Construct series connected two NMOS inverter logic gates using the N1 and N2 MOSFETs in the CD4007C package and the resistor value you calculated in task 2(i). Measure the voltage transfer characteristic of the first stage. Determine the V_{in} for which $V_{out} = V_{DD}/2$. Measure the transient characteristics of the first stage. Do the rise and fall times match your simulation? Measure the DC power consumption for '0' and '1' logic outputs.

6. ***CMOS Inverter Construction and Testing:*** Construct series connected three CMOS inverter logic gates with the CD4007C. Measure the voltage transfer characteristic of the first stage. Determine the V_{in} for which $V_{out} = V_{DD}/2$. Measure the transient characteristics of the first stage. Do the rise and fall times match your simulation? Measure the DC power consumption for '0' and '1' logic outputs.

7. ***Clock Generator Construction and Testing:*** Construct the CMOS Ring Oscillator and measure its output. Adjust the component values until the oscillation frequency falls within ±5% of your clock frequency. Determine the duty cycle of the resulting waveform. Does the signal reach the rails, i.e. 0V and 5V, or is it limited to some other values? Measure the power consumption of your circuit by measuring the average current drawn from the supply.

8. ***CMOS Two-Input Logic Gate Construction and Testing:*** *Odd numbered groups:* construct a NAND gate using the N1-P1 and N2-P2 pairs, and connect its output to the input of an inverter you implement with the N3-P3 pair. *Even numbered groups:* construct a NOR gate using the N1-P1 and N2-P2 pairs, and connect its output to the input of an inverter you implement with the N3-P3 pair. Both groups: measure the output of the first gate and the following inverter for all combinations of high and low inputs at your two input terminals to prove the functionality of your design.

9. ***Report and Demonstration:***
   - Your *full* report should clearly describe your design process, and present your theoretical, simulated, and experimental results. All lab partners should collaborate in the writing of the report.
   - Your *draft report* should be submitted to your TA electronically as a PDF file by Monday, 30 October 2017 at 2:00 PM. The TA will comment on your report by Wednesday, 1 November 2017 at 2:00 PM.
   - The *final report* for this task should be submitted to your TA electronically as a PDF file by Friday, 3 November 2017 at 2:00 PM. Make sure that you make necessary corrections as indicated by Prof. Payne as well as the TAs.
   - You'll be asked to schedule a short demonstration of your amplifier in the week of the due date. Each lab partner will be asked to reproduce a measurement from the report, and show where the measurement and measurement technique was recorded in their lab notebook. (Lab partners each receive a separate grade.)

Hints and tips:

1. At this stage, concentrate on obtaining a signal oscillating at the correct frequency. A method to obtain a 50% duty cycle square wave from the oscillator output will be implemented in Lab 4.
2. In principle, all three capacitors in the ring oscillator should have the same value. In practice, this is not necessary, but will result in a distorted output waveform. This distortion will be corrected in Lab 4.

References:

[1] A.S. Sedra, K.C. Smith, *Microelectronic Circuits*, 7th. Ed., New York, NY, Oxford University Press, 2015, ISBN 978-0-19-933913-6

[2] CD4007C data sheet, Fairchild Semiconductor, 2002

Time Management and Lab Notebook Documentation
ECE 342 Fall 2017 Lab 3

Group #_____ Names:_____

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Use this form to collect signatures from the TA as you complete the tasks below. Signatures must be collected on or before the due date. Include this completed form with your lab notebooks and final lab report.

Friday 13 October	**Attend the lab briefing and review the deadlines given below**. Any modifications must be approved by Wednesday, 4:00p.m.
Thursday 19 October 4:50 PM	***(10 pts)*** **Circuit design and simulation results completed.** All designs must be entered into lab notebooks *TA's: Rate from 1(worst) to 5 (best)...* Clarity of Design Process: 1 2 3 4 5 Lab Notebook Procedures: 1 2 3 4 5 Simulations Completed: 1 2 3 4 5 Clarity of Simulation Results: 1 2 3 4 5 Successful Design Complete: 1 2 3 4 5 Early Check-off: 1 2 3 4 5 Signature: Date:
Thursday 26 October 4:50 PM	***(10 pts)*** **Experimental measurements completed and entered into lab notebooks.** *TA's: Rate from 1(worst) to 5 (best)...* Experimental Procedures Clearly Described: 1 2 3 4 5 Lab Notebook Procedures: 1 2 3 4 5 Preliminary Analysis of Results: 1 2 3 4 5 Clarity of Results Presentation: 1 2 3 4 5 Successful Design Demonstrated: 1 2 3 4 5 Early Check-Off: 1 2 3 4 5 Signature: Date:
Monday 30 October 2:00 PM	***(10 pts)*** **Rough draft of report completed by 2:00 PM**. Text should be complete, requiring editing primarily for grammar, consistency, or presentation Signature: Date:
As Scheduled:	***(30 pts)*** **Demonstration:** Reproduce a measurement from your report for a grader. Expect to show the grader where the requested measurement and measurement technique was recorded in your notebook.
Friday 3 November 2:00 PM	***(40 pts)*** **Final Report Due, 2:00 PM.** Turn in your final report with this form. Reports are not accepted late.