ECE 342 Optical Link Project

LAB 3: MOSFET BASED LOGIC GATES AND THE DIGITAL OSCILLATOR

Function in the Optical Link Project

- The first stage in the transmitter generates a 20 kHz square wave signal with a 5 V amplitude.
- This is accomplished by using a digital oscillator.
  - Ring oscillator or astable multivibrator
- The digital oscillator will be built using three inverters connected in series, with the output of the last stage connected to the input of the first stage.
- A 555 timer or similar circuit would have made more sense, but the purpose of this module is to demonstrate MOSFET based logic gates.

Lab Objectives

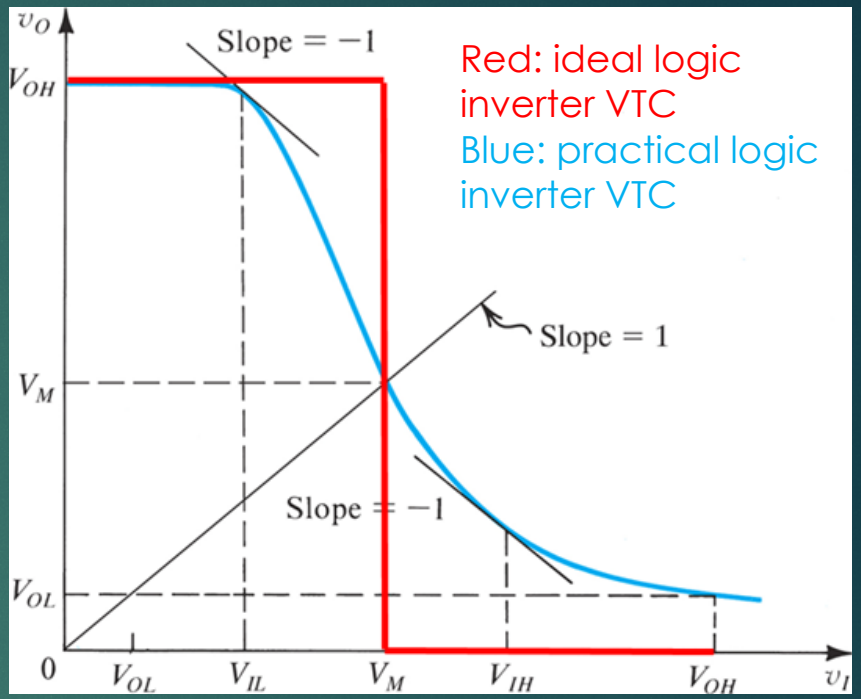
- Investigate the performance of MOSFET based logic gates
- Design a CMOS inverter based digital oscillator that will be used to generate the clock signal

MOSFET Based Logic Gates

- 99% or more of logic gates today are based on metal-oxide-semiconductor field-effect-transistors (MOSFETs)
- The basic MOSFET inverter circuit is the resistive load MOSFET inverter
  - Actually a common-source amplifier
- The most commonly used MOSFET inverter circuit is the complementary MOSFET (CMOS) inverter
  - Uses a p-channel and an n-channel MOSFET
- The basic inverter circuits can be extended to have multiple inputs and thus realize NAND or NOR logic gates

Logic Inverter VTC

- V_{OL}: Output low-level
- V_{OH}: Output high-level
- V_{IL}: maximum value of input voltage considered to be "logic low" level
- V_{OL}: minimum value of input voltage considered to be "logic high" level
- NM_L: Noise margin for logic low input
  - $NM_L = V_{IL}-V_{OL}$
- NM_H: Noise margin for logic high input
  - $NM_H = V_{OH}-V_{IH}$
- Usually, "logic high" = 1, "logic low" = 0

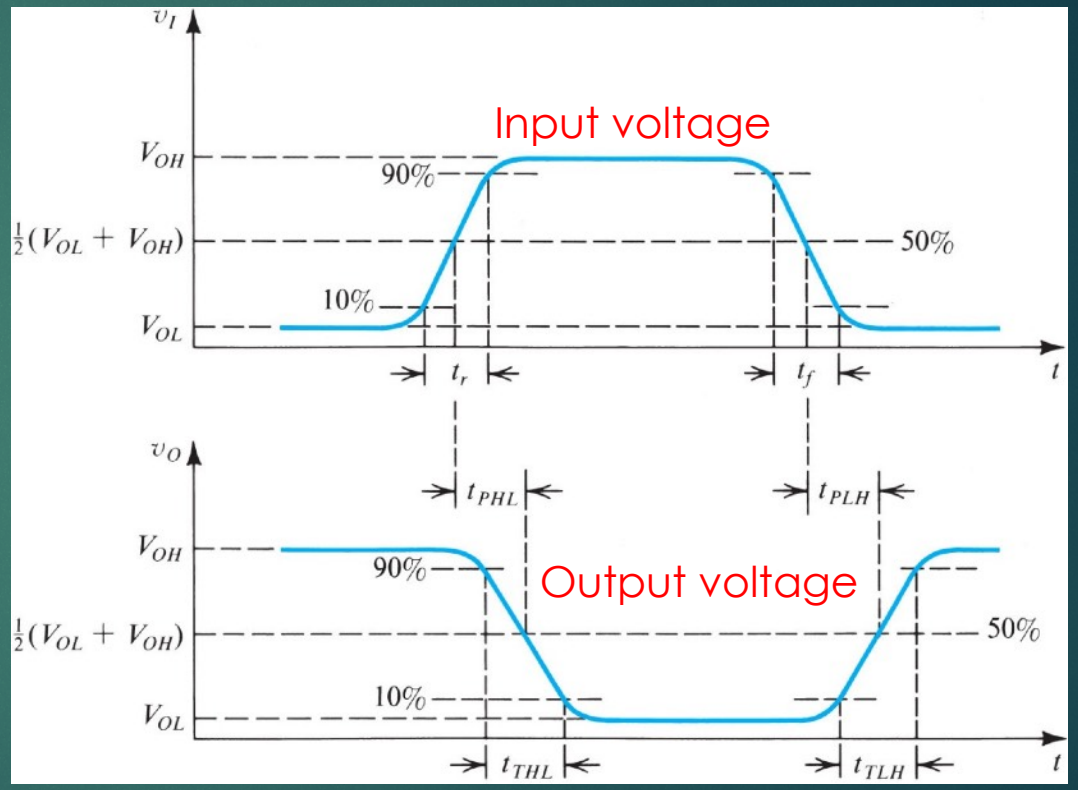


Voltage transfer characteristic of a resistive load NMOS logic inverter

Sedra & Smith, Fig. 14.15, augmented to show ideal VTC

Transient Characteristics of Logic Gates: Inverters

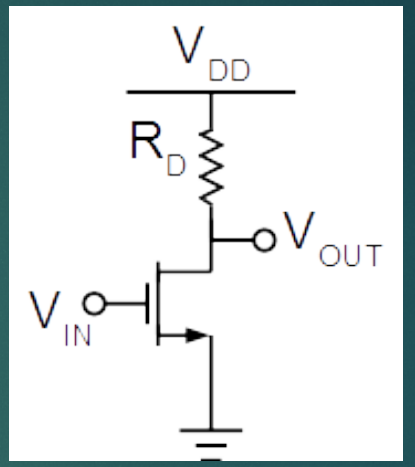
- Rise time: 10% → 90%
- Fall time: 90% → 10%
- Propagation delay: from 50% of input to 50% of output
  - The high-to-low and low-to-high transition delays can be different

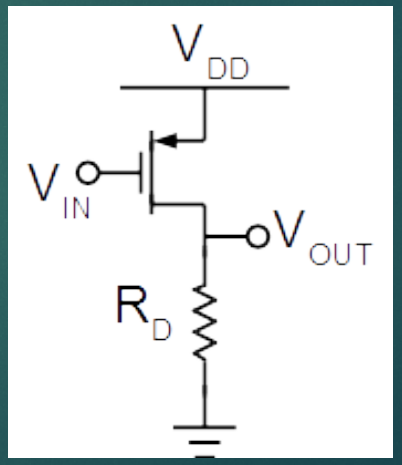


Sedra & Smith, Fig. 14.29

Resistive Load MOSFET Inverter

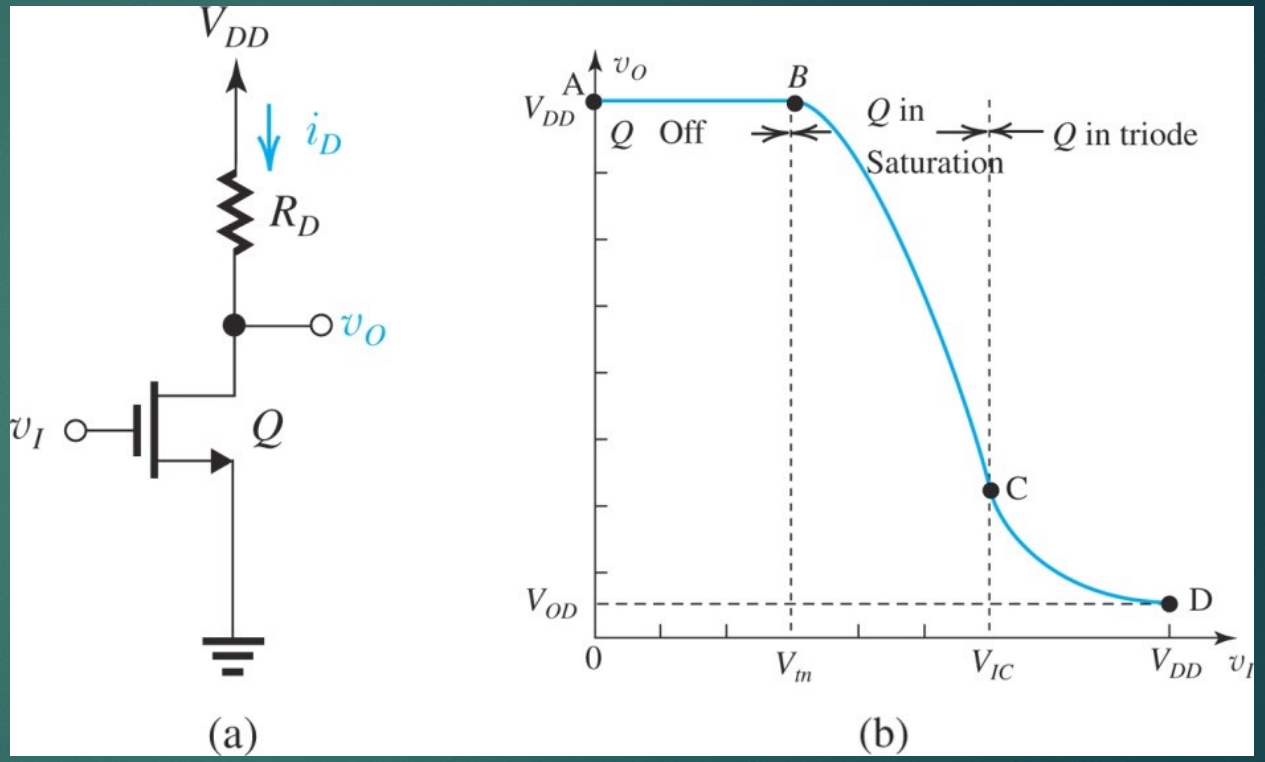
- The basic common source amplifier is also a logic inverter
- Consists of a MOSFET with a load resistor
- Can be based on a PMOS or NMOS FET
- Typically drives another MOSFET gate, i.e. a capacitive load





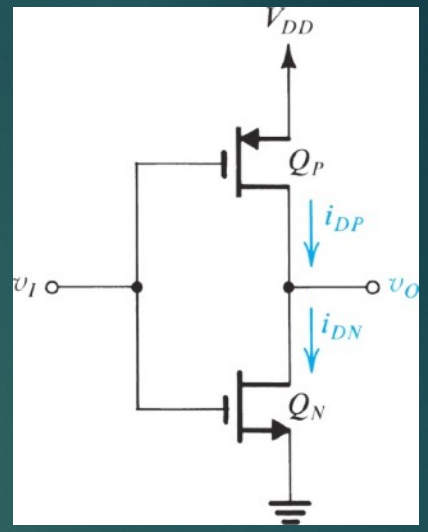
NMOS Resistive Load Inverter

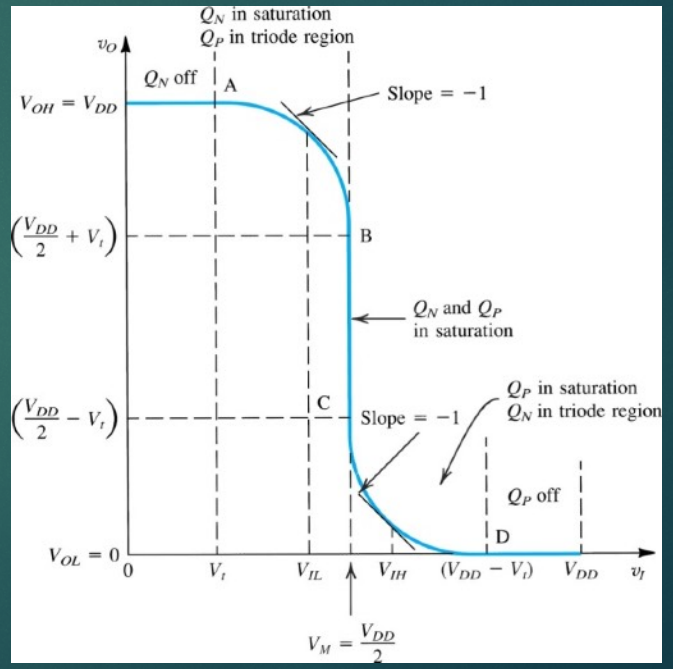
- For $V_{IN} < V_{tn}$:
  - The MOSFET is off
  - No current flows through R_D
  - $V_{OUT} = V_{DD}$
  - $I_{DS} = 0\ A \Rightarrow P = V_{DD}I_{DS} = 0\ W!$
- For $V_{IN} > V_{IH}$:
  - The MOSFET is in triode
  - $V_{OUT} = V_{DD} - I_{DS}R_D$
  - $P = V_{DD}I_{DS} \neq 0\ W!$
- Output characteristic is a function of both the MOSFET and R_D



CMOS Inverter

- For $V_{IN} < V_{t,n}$:
  - The NMOS is off, the PMOS is on
  - As no current flows, the voltage drop across the PMOS is 0 V
  - $V_{OUT} = V_{DD}$
- For $V_{IN} > V_{DD} + V_{t,p}$ ($V_{t,p} < 0$):
  - The PMOS is off, the NMOS is on
  - As no current flows, the voltage drop across the NMOS is 0 V
  - V_{OUT} = GND



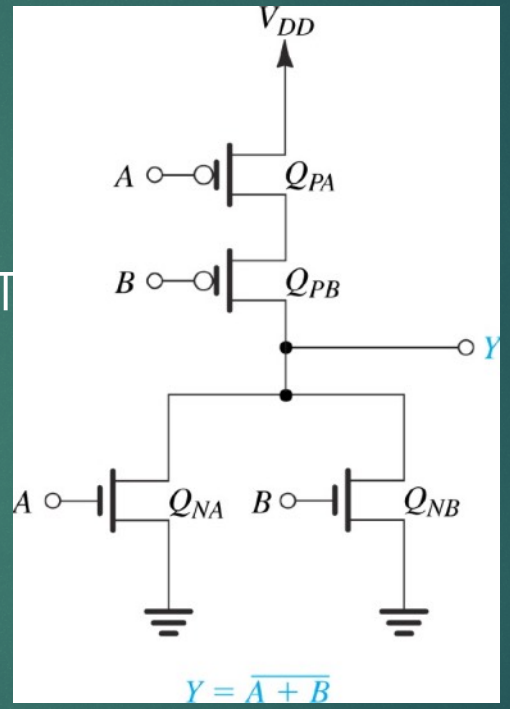


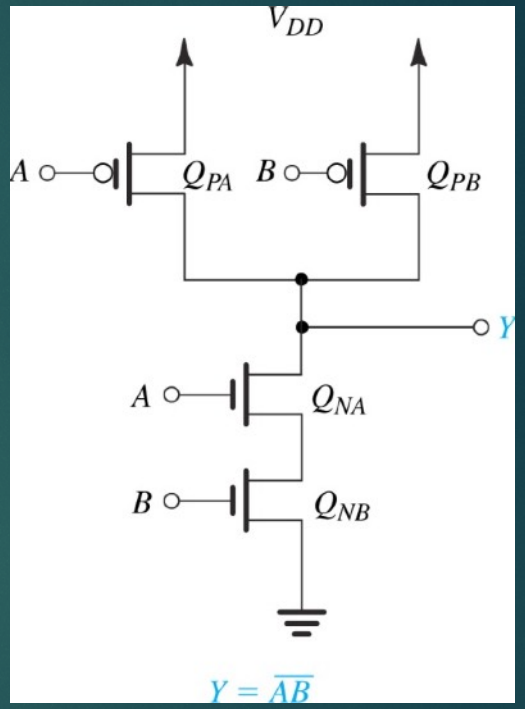
CMOS vs. Resistive Load Inverter

- The CMOS inverter has a DC power consumption advantage
  - The resistive load inverter consumes DC power
  - The CMOS inverter does not consume DC power
- The CMOS inverter VTC is more symmetric than the resistive load inverter
- The CMOS inverter typically has better noise margins

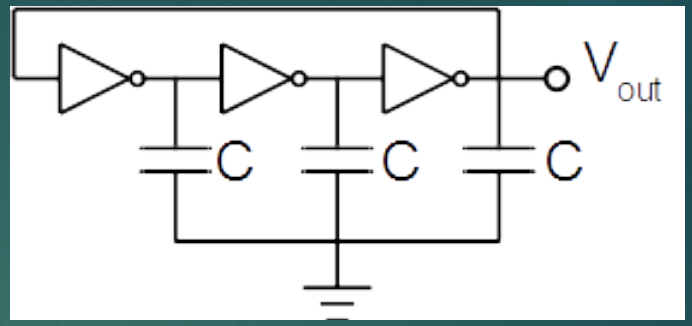
Two Input CMOS Logic Gates

- Deriving two-input logic gates is straight forward
- NMOS FETs in parallel implement the NOR function
  - The output goes to GND if any NMOS FET is on
- NMOS FETs in series implement the NAND function
  - The output goes to GND if all NMOS FETs are on
- The PMOS FETs need to be connected in the opposite manner



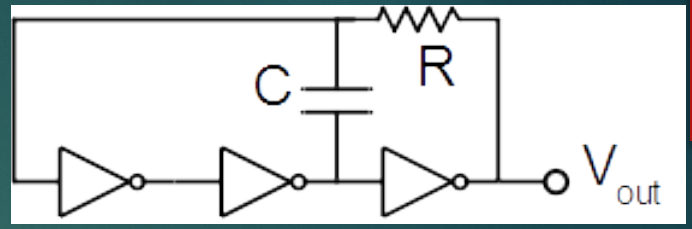


The Ring Oscillator



- An oscillator is obtained whenever an odd number of inverters are connected in series and the output is fed back to the input of the first inverter
- Used to demonstrate how fast a MOSFET technology can perform
- Ring oscillators on ICs use 127 or even 255 inverters!
- Need to use external capacitors to set the propagation delay for only three inverters
- Duty ratio and output voltage limits may be non-ideal

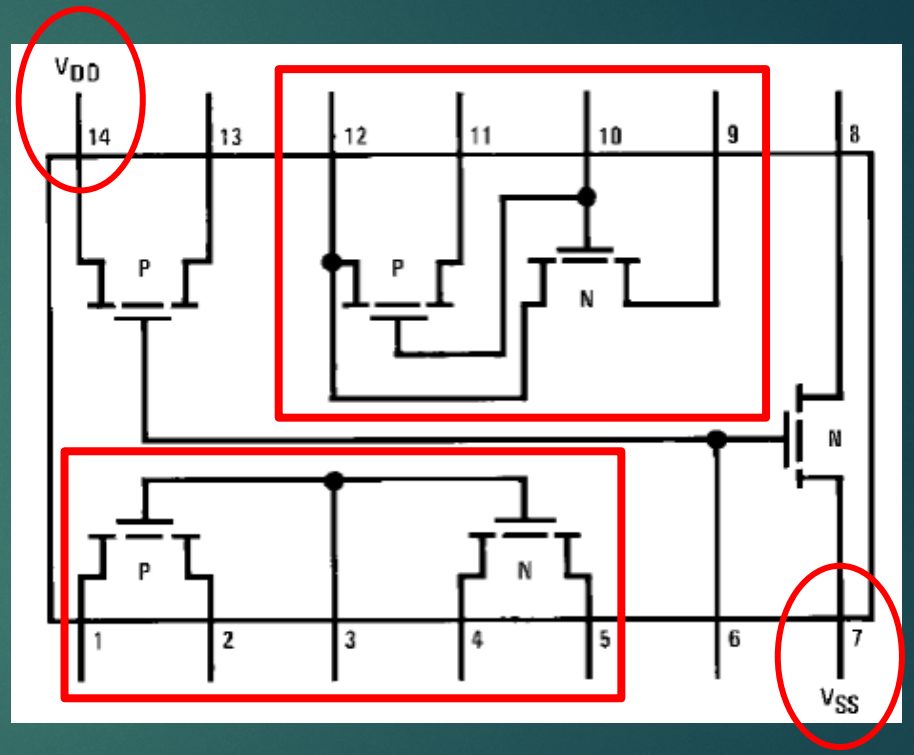
The Astable Multivibrator



- An RC network is used to connect the output back to the input
- The output is nearly a perfect wave, if taken from the correct inverter
- The duty cycle is approximately 50%
- Only two external components are needed to set the clock frequency
  - One is a resistor

The CD4007 Integrated Circuit

- Contains three CMOS pairs
- Pair N1-P1 S terminals are connected to the supply pins
- The PMOS bodies are connected to V_{DD}
- The NMOS bodies are connected to V_{SS}
- Pair N2-P2 S & D are determined by the circuit connection (pins 1-5)
- One pair is configured as an inverter (pins 9-12)
- $V_{DD} - V_{SS} \leq 15$ V
- Be careful when connecting the S & D pins



Tasks: Overview

- The first task is to investigate the NMOS resistive load inverter
  - How does the drain resistor impact output voltage (V_{OL}), DC power consumption ($P_{DC} = V_{OL}xI_{DS}$) and response time?
- The second task is to study to CMOS inverter
- The third task is to design a clock generator circuit for the project
  - Investigate and compare a ring oscillator with an astable multivibrator through simulation
  - Choose one to build and test for the project
- The fourth task is to study two-input CMOS logic gates

Tasks: NMOS Inverter Simulation

- Calculate the value of R_D that will give V_{OUT} = 2.5 V for V_{IN} = 2.5 V
- Simulate V_{OL} vs. R_D, for R_D = 1 kΩ to 100 kΩ
- Simulate and plot the VTC for R_D = 1 kΩ, 100 kΩ and the value you calculated
  - Driving an identical NMOS inverter
  - Determine the power consumption
- Simulate the transient characteristics for R_D = 1 kΩ, 100 kΩ and the value you calculated
  - Driving an identical NMOS inverter
  - 10 pF capacitor to model breadboard
- Repeat transient for calculated R_D only for V_{DD} = 10 V and 15V

Tasks: NMOS Inverter Build & Test

- Build two NMOS resistive load inverters using the drain resistor value you calculated
- Measure VTC
- Measure the transient response
- Measure the DC power consumption for logic low (V_{IN}=0) and logic high (V_{IN}=V_{DD}) inputs

Task: Two Input Logic Gates

- Even though this task is listed last in the manual, you should do it before the CMOS inverter and clock generator experiments to minimize your setup times
- Odd numbered groups construct a NAND gate, and connect its output to the input of an inverter
- Even numbered groups construct a NOR gate, and connect its output to the input of an inverter
- Measure the output of the first gate and the following inverter for all combinations of high and low inputs at your two input terminals to prove the functionality of your circuit

Task: CMOS Inverter

- Simulate the CMOS inverter by connecting three inverters in series
  - VTC of the first inverter
  - Rise and fall times
  - Propagation delay
- Build three CMOS inverters in series and measure:
  - VTC of the first inverter
  - Rise and fall times
  - Propagation delay
  - DC power consumption for logic low and logic high inputs

Task: Clock Generator

- Simulate the ring oscillator and astable multivibrator
  - Determine the external capacitors needed to set the clock frequency of the ring oscillator
  - Determine the R and C needed to set the clock frequency of the astable multivibrator
- Choose one to build and test
- Build chosen design
  - Adjust the component values until the oscillation frequency falls within ±5% of your clock frequency
  - Determine the duty cycle of the resulting waveform
  - Measure the power consumption of your circuit by measuring the average current drawn from the supply

Tips and Tricks

- This task has lots of simulations to do, but the experiments are short
- A methodical approach to doing the simulations can speed up the process
- For example, you can simulate multiple VTCs at once by using (i) two variables instead of one, or (ii) the Stepping function during the DC simulation
- Carrying out the experiments in the presented order will be efficient time-wise