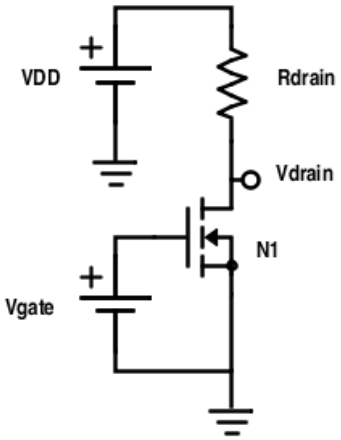
Solving the Output Voltage of a Resistively Loaded MOSFET Logic Gate

A. Solving the Output Voltages for Logic 0 and Logic 1 Inputs



The figure above shows a resistively loaded NMOS inverter logic gate, constructed with an enhancement mode MOSFET, as used in Task 3. There are two extremes that need to be considered for logic operations:

- Logic 0 input: V_{gate} = 0 V, and the logic 1 output will be $V_{drain} = V_{DD}$.
- Logic 1 input: $V_{gate} = V_{DD}$, and the logic 0 output will be V_{drain} = 0 V.

The first, logic 0 input / logic 1 output, corresponds to no current flowing through the circuit, and the MOSFET is operating in cut-off, i.e. it is off.

Cut-off: $|V_{GS}| < |V_t|$ $I_{DS} = 0$

The second, logic 1 input / logic 0, corresponds to the MOSFET operating in the triode regions, as $V_{gate} = V_{DD}$ but $V_{drain} \cong 0$ V, therefore $V_{DS} < V_{GS}-V_t$. For an NMOS, this gives:

Triode: $|V_{GS}| < |V_t|$ and $|V_{DS}| < |V_{GS}-V_t|$

$$I_{DS} = \mu_n C_{ox} \frac{W}{L}\left[\left(V_{GS} - V_t\right)V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

Calculating the output voltage for a logic 1 input requires solving two coupled equations. The current through the drain resistor, I_R, is equal to the drain current, I_{DS}, of the NMOS FET. The current across the resistor is:

$$I_R = \frac{V_{DD} - V_{DS}}{R_{drain}} \qquad (Eq.\,1)$$

The drain current is:

$$I_{DS} = \mu_n C_{ox} \frac{W}{L}\left[\left(V_{GS} - V_t\right)V_{DS} - \frac{1}{2}V_{DS}^2\right] \qquad (Eq.\,2)$$

Equating the two currents gives:

$$\frac{V_{DD}-V_{DS}}{R_{drain}}=\mu_n C_{ox}\frac{W}{L}\left[\left(V_{GS}-V_t\right)V_{DS}-\frac{1}{2}V_{DS}^2\right]$$

Defining k = $R_{drain}\mu_n C_{ox}\frac{W}{L}$, we can re-write the equation as:

$$\frac{k}{2}V_{DS}^2-\left[k\left(V_{GS}-V_t\right)+1\right]V_{DS}+V_{DD}=0 \qquad (Eq.3)$$

The two roots for an equation in the form of $ax^2 + bx + c = 0$ are $x_{1,2}=\frac{-b\pm\sqrt{\Delta}}{2a}$

where $\Delta = b^2-4ac$. Only one of the two roots will be physically meaningful and therefore the correct solution. To be meaningful, the correct root for V_{DS} should ensure the device is operating (i) within the supply voltage limits, and (ii) the MOSFET is operating in the triode region.

Example 1. Solving for the logic 0 and logic 1 output levels

As an example, lets assume V_{DD} = 5 V, R_{drain} = 20 kΩ, and that the NMOS FET has $\mu_n C_{ox}\frac{W}{L}=1\ \frac{mA}{V^2}$ and $V_{t,n}$ = 1 V.

- The output for Logic 0 input, i.e. Logic 1 output is Vout = Vdrain = V_{DD} = 5 V.
- What about the output for Logic 1 input? We can either use equation (3), or solve the two equations explicitly.

The current across the resistor is:

$$I_R=\frac{V_{DD}-V_{DS}}{R_{drain}}=\frac{5-V_{DS}}{20,000}$$

The drain current is:

$$I_{DS}=\mu_n C_{ox}\frac{W}{L}\left[\left(V_{GS}-V_t\right)V_{DS}-\frac{1}{2}V_{DS}^2\right]=1\times10^{-3}\times\left[\left(5-1\right)V_{DS}-0.5V_{DS}^2\right]$$

$$I_{DS}=10^{-3}\times\left[4V_{DS}-0.5V_{DS}^2\right]$$

So when we equate the two:

$$\frac{5-V_{DS}}{20,000}=10^{-3}\times\left[4V_{DS}-0.5V_{DS}^2\right]$$

$$5-V_{DS}=20\times\left[4V_{DS}-0.5V_{DS}^2\right]$$

Hence, we will obtain:

$$10V_{DS}^2-81V_{DS}+5=0$$

Solving for the roots give: V_{DS1} = 8 V and V_{DS2} = 62 mV.
The first root is not physically meaningful, as (i) it is larger than the supply voltage, and

(ii) would result in $V_{DS} > V_{GS-Vt}$, i.e. operation in the saturation mode instead of the in triode mode.

The physically meaningful root is $V_{drain} = V_{DS2} = 62$ mV.

So a logic 0 output for this circuit is 62 mV.

B. Solving for an Arbitrary Input & Output Voltage Combination

One of the design sub-tasks in Task 3 is to determine the drain resistor value that will result in $V_{out} = 2.5$ V when $V_{in} = 2.5$. To proceed with the solution, we need to determine if the MOSFET is operating in triode or saturation. Realizing that $V_{out} = V_{DS}$ and $V_{IN} = V_{GS}$, we have:

- $V_{GS} = 2.5\text{ V} > V_t = 1\text{ V}$, so the MOSFET is on, operating either in triode or saturation.
- $V_{DS} = 2.5\text{ V} > V_{GS} - V_t = 1.5$ V. So the MOSFET is operating in saturation.

The MOSFET I-V characteristic for operation in saturation is:

$$I_{DS} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)\left(V_{GS} - V_t\right)^2 \qquad (Eq.4)$$

A more accurate version of this equation that accounts for the channel length effect includes a V_{DS} term as well. We will ignore that additional term for now.

Plugging in the parameters, we obtain:

$I_{DS} = 0.5 \text{ x } 1\text{ mA/V}^2 \text{ x } (2.5 - 1)^2 = 1.125$ mA

The resistor can be solved using:

$$R_{drain} = \frac{V_{DD} - V_{DS}}{I_R} = \frac{5 - 2.5}{1.125\,mA} = 2222\ \Omega$$

Using the 5% tolerance resistor available in the parts store, we would choose $R_{drain} = 2.2$ kΩ.

For the CD4007UBE NMOS FET used in Task 3:

$$\mu_n C_{ox}\left(\frac{W}{L}\right) \cong 500\frac{\mu A}{V^2}$$

$V_{tn} = 0.95\text{ V} \cong 1\text{ V}$