ECE 342 Fall 2017 Optoelectronic Link Project

Lab 5: NMOS Common Source and NPN BJT Common Emitter Amplifiers

Overview

The final stage of the receiver circuit will be an amplifier circuit implemented with n-type MOSFETs (NMOS transistors) or bipolar junction transistors (BJTs). We expect the output of the active bandpass filter output to be in the hundreds of mV to low V range. The purpose of this amplifier will stage will be to increase this signal level to 5V.

NMOS Common Source Amplifier

A common source amplifier with a current sink for setting the bias current is shown in figure 1. Transistor N_1 is used for the common source amplifier, while the pair N_2 – N_3 forms a current sink to bias N_1. The gate resistor R_G should have a large value, and is used to ensure a DC bias of 0V at the gate of N_1. The resistors R_D and R_S are used to set the appropriate bias voltages at the drain and source terminals. The coupling capacitors C_G and C_D are used to ensure the gate and drain terminals are isolated from the input and output, respectively, under DC conditions. The bypass capacitor C_S ensures that the source terminal is essentially grounded at the signal frequencies.

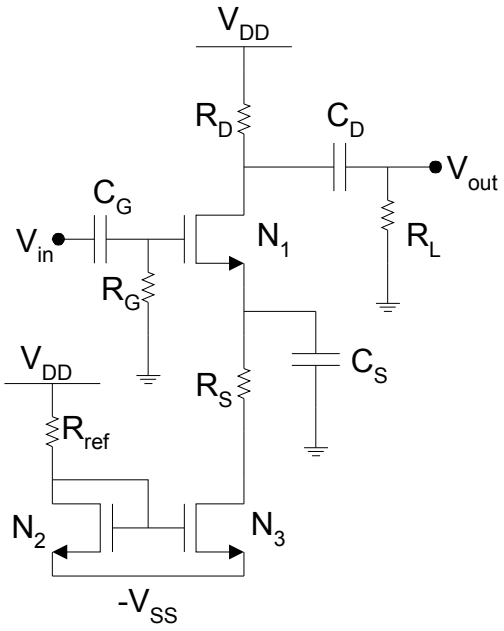

Figure 1. NMOS common source amplifier with current sink for biasing.

The source and body terminals of the 2N7000 MOSFET are internally connected, hence the body effect can be neglected. You should remember to tie the body terminal to the source terminal when you do the MicroCap simulations. The purpose of the resistor R_S connected between the source of N_1 and the drain of N_3 is to limit the channel length modulation effect on N_3. Ideally, the drain of N_3 should be at the same potential as N_2, for the two transistors to conduct the same current. However, if N_3's drain is connected to N_1's source, it will conduct a larger current than N_2 due to the channel length modulation effect.

The specifications for the amplifier circuit you will design for this lab experiment are given in Table 1. The load resistance R_L is specified to be 1 kΩ or 1 MΩ. The larger value is consistent with the input resistance of most analog-to-digital converter (ADC) circuits, such as those in the Digilent Analog Discovery unit. The specificiation for the second harmonic distortion essentially means that you should bias your circuit (i.e. choose R_D) such that your output signal should be very symmetric when you have a 20 mVp-p sinusoidal input signal, i.e. very little clipping occurs. The 200 kHz upper cut-off frequency specification is due to the fact that the output of this circuit should ideally be a square wave when connected to the rest of the receiver circuit.

Table 1. NMOS common source amplifier specifications:

MOSFETs N_1, N_2, N_3	2N7000
Load resistance, R_L	1 kΩ[1] and 1 MΩ[2]
Peak gain, with load	21 dB ± 1 dB
Bias current for N_1	~ 1 mA
Lower cut-off frequency	< 1 kHz
Upper cut-off frequency	At least 200 kHz
R_{in}, small signal	At least 1 MΩ
R_{out}, small signal	At least 3 kΩ
2nd Harmonic distortion for 20 mV_{p-p} sinusoidal signal at 1 kHz[3]	< 2%
Supply voltages	±12 V

[1] For use as a generic analog amplifier
[2] For use as the final stage of the optical link receiver
[3] This specification is valid for R_L = 1kΩ

An important consideration for the amplifier as given is that its output voltage swing will be significantly larger than $5V_{p-p}$. The upper limit at the drain of N_1 is V_{DD} = +12V. You will calculate the lower limit at the drain of N_1 as part of your design.

NPN BJT Common Emitter Amplifier

A BJT common emitter amplifier circuit is shown in figure 2. The circuit operates in a similar manner to the NMOS CS amplifier in figure 1. Transistor Q_1 is the amplifier, while the transistor pair Q_2 and Q_3 forms a current sink. The resistor values in the circuit are chosen so that the collector current of the BJT is 1 mA, which is the approximate drain current of the CS amplifier you are to design. Note that the resistor values are not necessarily the same for the two circuits. The component values are given in Table 2.

Table 2. NPN common emitter amplifier component values:

Q1, Q2, Q3	2N3904
R_{ref}	19.3 kΩ

R_C	4.7 kΩ
R_B	10 kΩ
R_E	3.3 kΩ
R_L	1 kΩ
C_B, C_C, C_E	< 1 μF

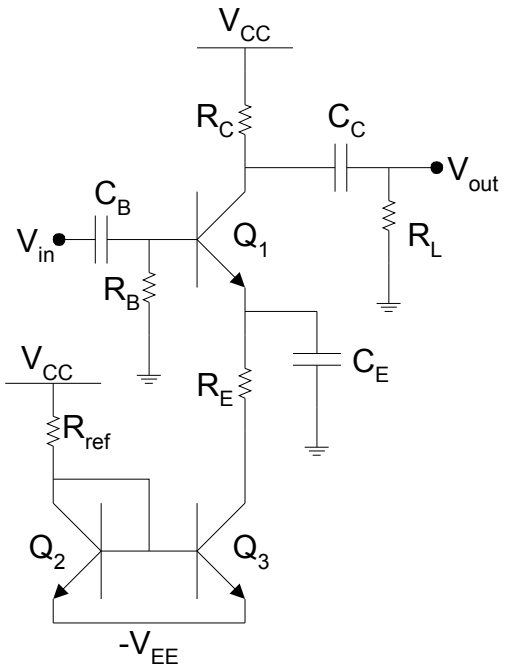

Figure 2. NPN BJT common emitter amplifier with current sink for biasing the amplifier.

Comparison of the BJT and MOSFET for amplifiers

The BJT is a current-to-current amplifier, while the MOSFET is a voltage-to-current amplifier, i.e. a transconductance amplifier. The input current into the base terminal of the BJT controls the current flowing from the collector to the emitter. We can still model the BJT as a transconductance amplifier, by modeling the input current-voltage relationship appropriately. The bipolar junction transistor (BJT) is preferred for analog circuit design for its larger transconductance, which depends only on the collector bias current I_C, and resulting larger current handling capacity.

A further advantage of BJTs is that they usually have a smaller noise figure than MOSFETs, i.e. they are less noisy. This is because the transistor action in the BJTs occur in the bulk of the Si crystal, while the transistor action in the MOSFETs occur at the Si crystal's surface. The defect density at the surface of any crystal is likely to orders of magnitude larger than the bulk of the crystal. Therefore, there are many electrically traps at the surface, creating random generation-recombination events which show up as noise. In this particular experiment, the MOSFET is a 2N7000 power transistor while the NPN is a 2N3904 small-signal transistor. Power transistors are optimized for power handling, not low noise.

An important difference between BJTs and MOSFETs is that the BJT is a bipolar device, while the MOSFET is a unipolar device. That is, both electrons and holes conduct in a BJT, while only electrons or

only holes conduct current in a MOSFET. Furthermore, the MOSFET is a symmetric device, and S and D terminals are determined by how the device is connected in a circuit. The BJT is an asymmetric device, with the emitter being the highest doped region and the collector being the lowest doped region in the device. It is possible to operate a BJT in reverse, but this will result in signal attenuation instead of gain!

Tasks

1. ***NMOS common source amplifier design:*** Complete the design of NMOS CS amplifier circuit given in figure 1 to meet the specifications given in Table 1. Show the details of your calculations and explain your reasoning for your design choices. Use DC analysis to determine your bias component values and small signal analysis to calculate the input resistance, output resistance, and open-circuit voltage gain A_{vo} of your design, i.e. the gain without R_L. Propose a method to limit the voltage swing at the output (V_{out}) between -1V and +5.5V
2. ***NMOS CS amplifier simulation:*** Simulate the circuit you designed and refine your design until you meet specifications. Explain, or at least speculate on, the reasons for any significant deviations from your design values. What is the actual open circuit voltage gain of your circuit, i.e. the gain without R_L? You will need to do AC simulations for the gain vs. frequency plots, and a transient simulation to verify the 2nd harmonic distortion spec. The latter should be done only for the loaded circuit, i.e. with the capacitively coupled 1 kΩ load attached to the circuit.
3. ***BJT CE amplifier simulation:*** Do the same simulations in task 2 for the BJT CE amplifier circuit shown in figure 2, with the values given in table 2. How does this circuit compare with the NMOS CS amplifier?
4. ***NMOS CS amplifier construction and testing:*** Construct and test your amplifier design. Measure the DC bias voltage values, the gain from 100 Hz to 1 MHz, and the low-frequency cut-off. If you have to, tweak your design until you meet specifications. Determine the 3 dB bandwidth and pass-band ripple.
5. ***BJT CE amplifier construction and testing:*** Construct the NPN CE amplifier circuit shown in figure 3. Measure DC bias voltage values, the gain from 100 Hz to 1 MHz, and the low-frequency cut-off. Determine the 3 dB bandwidth, and pass band ripple.
6. ***Choosing the final stage amplifier:*** Test your optoelectronic link project with the CS and the CE amplifier as the output stage at a fixed distance (e.g. 30 feet). Which amplifier gave a better result in terms of signal-to-noise ration, SNR? Can you determine why? Choose the best performing amplifier and use it as the final stage of the receiver module for your optoelectronic link final demonstration.
7. ***Report and Demonstration***
   - Your *full* report should clearly describe your design process, and present your theoretical, simulated, and experimental results. All lab partners should collaborate in the writing of the report.
   - Your *draft report* should be submitted to your TA electronically as a PDF file by Monday 4 December 2017 at 2:00 PM. The TA will comment on your report by Wednesday 6 December 2017 at 2:00 PM.
   - The *final report* for this task should be submitted to your TA electronically as a PDF file by Friday, 8 December 2017 at 2:00 PM. Make sure that you make necessary corrections as indicated by Prof. Payne as well as the TAs.
   - You'll be asked to schedule a short demonstration of your amplifier in the week of the due date. Each lab partner will be asked to reproduce a measurement from the report, and show where the measurement and measurement technique was recorded in their lab notebook. (Lab partners each receive a separate grade.)

Time Management and Lab Notebook Documentation
ECE 342 Fall 2016 Lab 5

Group #_____ Names:_____

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The deadlines for Lab 5 are given below:

Wednesday 8 November	**Lab Briefing** - during class
Thursday 17 November 2017	***(10 pts)*** **Circuit design and simulation results completed.** All designs must be entered into lab notebooks *TA's: Rate from 1(worst) to 5 (best)...* Clarity of Design Process: 1 2 3 4 5 Lab Notebook Procedures: 1 2 3 4 5 Simulations Completed: 1 2 3 4 5 Clarity of Simulation Results: 1 2 3 4 5 Successful Design Complete: 1 2 3 4 5 Early Check-off: 1 2 3 4 5 Signature: Date:
Thursday 30 November 2017	***(10 pts)*** **Experimental measurements completed and entered into lab notebooks.** *TA's: Rate from 1(worst) to 5 (best)...* Experimental Procedures Clearly Described: 1 2 3 4 5 Lab Notebook Procedures: 1 2 3 4 5 Preliminary Analysis of Results: 1 2 3 4 5 Clarity of Results Presentation: 1 2 3 4 5 Successful Design Demonstrated: 1 2 3 4 5 Early Check-Off: 1 2 3 4 5 Signature: Date:
Monday 4 December 2017	***(10 pts)*** **Rough draft of report completed by 2:00 PM**. Text should be complete, requiring editing primarily for grammar, consistency, or presentation. Submit as a PDF file.
As Scheduled:	***(30 pts)*** **Demonstration:** Reproduce a measurement from your report for a grader. Expect to show the grader where the requested measurement and measurement technique was recorded in your notebook.
Friday 8 December 2017	***(40 pts)*** **Final Report Due, 2:00 PM.** Turn in your final task report as a PDF file. Reports are not accepted late.