320MHz RFID Mixer Design

ECE547 Final Report

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1 Introduction

1.1 Project Overview

There are many applications opening up in Radio Frequency Identification (RFID), such as tracking of a large number of products or counting of large number of identical items. They offer advantages over labels and bar-codes as the radio signal can penetrates dirt, moistures and even nonmetallic objects in a long distance. There are many reported literatures and results about passive RFID design [1], but not too many on active RFID, which finds its applications in temperature and moisture monitoring, products condition reporting among others. Those applications determine the structure of active tag different from that of passive one. It needs to have its own power supply, and more often, it should possess its own transceiver circuits.

This project is trying to design transmitter used in active RFID. The proposed structure consists of three parts like that in Fig. 1.1:

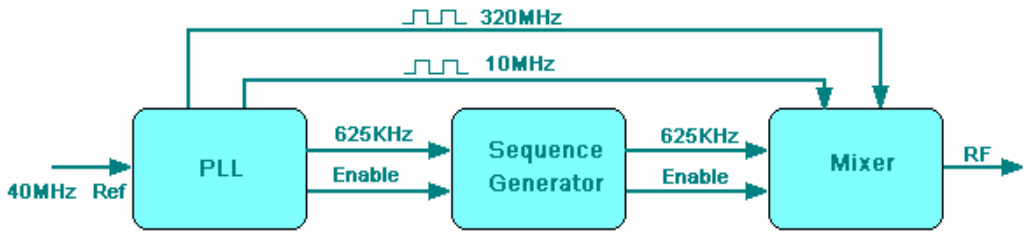

Fig.1.1 Transmitter in Active RFID

First part is Phase Locked Loop (PLL), which takes the 40MHz external reference clock to generate 320MHz carrier (LO) signal and 10 MHz intermediate frequency (IF) signal. Second is Sequence Generator, which takes 625 KHz signal as working clock signal and generates the bit sequence. This bit sequence will modulate the mixer's output. The modulation scheme chosen in this project is FSK. In this transmitter, the upconverting mixer is designed; the desired output signal's frequency of this mixer is 330MHz.

1.2 Project Objective

There are lots of literatures introducing passive RFID structures and addressing its design issues. But for the active RFID, there are fewer documents introducing its structure and how to design it. Because of the above reasons, this project is trying to design a high-frequency transmitter, which could be part of active RFID system. The transmitter structure proposed in this project can be a reference structure for the future RFID design. And some design issues that could

encounter in the future RFID design are addressed in this project.

My part of work in this project is to design the upconverting mixer and peripheral circuits. The input signals for this mixer are all digital versions signal-ended. So the design issue involves how to converter those single-ended signals to a suitable version, such as from single-ended to differential converting. Also the power consumption of the mixer is concerned.

1.3 Table Listing of Specifications

1.3.1 Design Specifications

Name	Specification
The carrier Frequency LO	320MHz
Intermediate Frequency (IF)	10MHz
Output Signal (RF) Frequency	330MHz
VSS	0V
VDD	5V

Table 1.1 Design Specifications

1.3.2 Testing Specifications

Name	Specification	Properties
The Carrier Frequency LO	50MHz~320MHz	Differential
Intermediate Frequency (IF)	1M~10MHz	Differential
VSS	0V	
VDD	5V	

Table 1.2 Testing Specifications

1.3.3 Table of Macros

Name	Function
Mixer_Biased	This is the upconverting mixer with biasing network, mixing 320MHz input carrier signal with 10MHz IF signal, and output 330MHz differential RF signal.
IF_Input	This block is to converter the 10MHz digital input signal to 10MHz sine waveform with magnitude less than 1V. Three order low pass filter is involved.
Single-to-Differential Converter	This block is to generate two differential output signals LO+ and LO- with anti-phase and magnitude less than 1V.
Diff-to-Single	The RF outputs of mixer are differential version, this block is to converter them into a single-ended signal
LO_Input	This block is to converter the 320MHz digital input signal to 320MHz sine wave. Two order low pass filter is designed.
Modulator	Inputs to this block are 330MHz, 320MHz signals and bit sequence. Bit sequence will modulate output between those two signals to implement FSK. Also this block provides buffering to drive large capacitive load for testing purpose. In real RFID this buffer is not necessary

Table 1.3 Lists of Macros

1.3.4 Table of Pins

1	LO+
2	LO-
3	IF+
4	IF-
17	Test_Out
19	gnd!
20	vdd!
27	IF
29	LO
32	vdd!
34	Out
35	gnd!
38	Bit_Seq
40	Gnd!

Table 1.4 Pin Assignments

2 Circuit Design

2.1 Mixer Design

The purpose of the mixer is to converter a signal from one frequency to another. In a transmitter, this conversion is from intermediate frequency to radio frequency. Mixing requires a circuit with nonlinear transfer function since nonlinearity is necessary to generate new frequency. The circuit to implement such nonlinearity can be as simple as a switch like that in Fig. 2.1. Its working principle is given as follows:

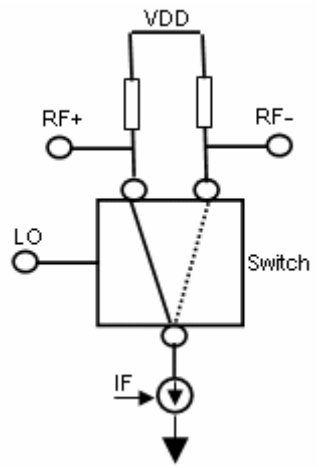

Fig. 2.1 Conceptual Schematic of Mixer

The input of the mixer is a gain stage. The amplified current from the gain stage is passed into the switching stage. This stage steers the current between the two differential outputs depending on the LO signal (a square wave). This steering has the effect of multiplying the current from the gain stage by +/-1. Thus it can be used to move the signal IF from one frequency to another according to the following deduction.

Assuming IF signal has the following form:

$$v_{IF}(t) = A_{IF}\sin(\varpi_{IF}t)$$

And the LO signal has the form of:

$$u(v_{LO}(t)) = \begin{cases} 1 & if \quad v_{LO}(t) > 0 \\ -1 & if \quad v_{LO}(t) < 0 \end{cases}$$

Further, $u(v_{LO}(t))$ can be expressed by a Fourier series:

$$u(v_{LO}(t)) = \frac{4}{\pi}\sin(\varpi_{LO}t) + \frac{4}{3\pi}\sin(3\varpi_{LO}t) + \frac{4}{5\pi}\sin(5\varpi_{LO}t) + ...$$

So the mixed output is:

$$\begin{aligned} v_{RF} &= v_{IF}(t) \cdot u(v_{LO}(t)) \\ &= A_{IF}\sin(\varpi_{IF}t)(\frac{4}{\pi}\sin(\varpi_{LO}t) + \frac{4}{3\pi}\sin(3\varpi_{LO}t) + \frac{4}{5\pi}\sin(5\varpi_{LO}t) + ...) \\ &= \frac{1}{2}\cdot\frac{4}{\pi}A_{IF}\sin[(\varpi_{IF} + \varpi_{LO})t] + \frac{1}{2}\cdot\frac{4}{\pi}A_{IF}\sin[(\varpi_{RF} - \varpi_{LO})t] + ... \end{aligned}$$

For the transmitter, the desired part is the first term in the above equation. Other harmonics are assumed to be filtered out by the following filter.

2.2 Mixer Topology

Passive mixers have higher linearity and better frequency response; but they do not have high gain. Let's consider the noise figure of a system consists of many components in series. The whole system's noise figure is given by the following formula.

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots$$

F_i and G_i are noise figure and gain of *ith* stage component. This formula shows the presence of gain preceding a stage causes the effective noise figure to be reduced compared to the measured noise figure of a stage by itself. High gain is preferred. That is the reason why passive mixer is not widely used. Active mixers have higher gain which contributes to noise reduction.

One simple active mixer is single-balanced mixer. Its basic structure is given in Fig. 2.2.

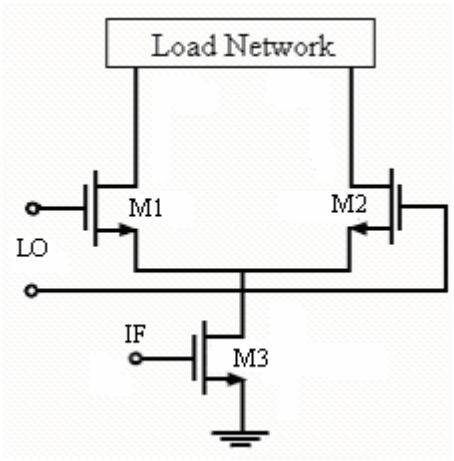

Fig. 2.2 Single-balanced mixer

It consists of a transconductance stage M3, switching stage of M1 and M2 and a load network. Transconductance stage results in a voltage-to-current conversion from V_{in} to drain current $g_m V_{in}$. Source degeneration may be added to improve linearity. This configuration has many drawbacks. It is susceptible to noise in the LO signal. LO signal can feed through to the output and the IF signals. All those make single-balanced mixer rarely used.

Double-balanced mixer are used to reduce the LO-feed through to IF and output. Its structure is like that in the Fig. 2.3.

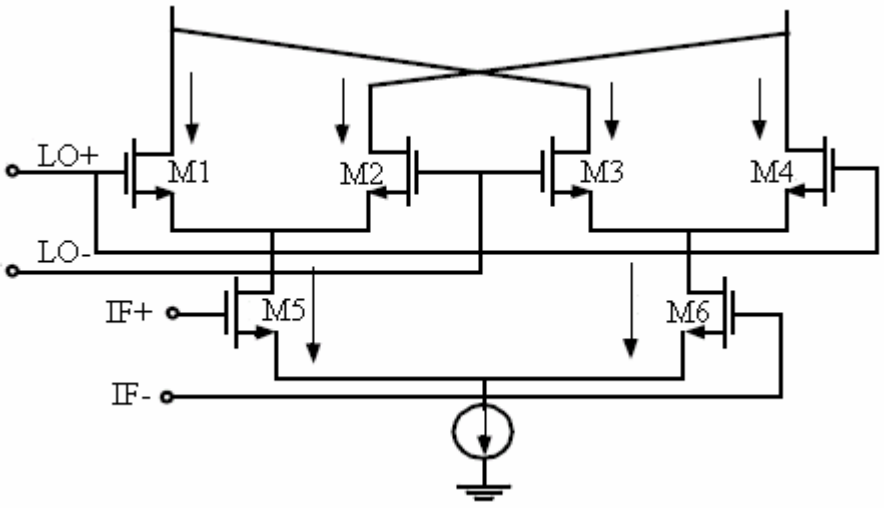

Fig. 2.3 Double-balanced Mixer

The two single-balanced mixers are connected in anti-parallel as far as the LO is concerned but in parallel for the IF signal. Therefore, the LO terms sum to zero in

the output, whereas the converted IF signal is doubled in the output. This mixer thus provides a high degree of LO-IF isolation, reduction of noise in the outputs, easing filtering requirement at the output.

2.3 Source Degeneration

One of the mixer's performance measurements is its linearity. There are several methods to improve mixer's linearity. Such as increasing supply voltage or biasing current. But all those will increase the mixer's power consumption. The most common way is to add source degeneration. Resistor or inductor can be used as source degeneration. Inductor degeneration has more advantage over resistor. It has no thermal noise to degrade the noise figure of mixer, and it has no DC voltage drop across it [2]. But we choose resistor in this design, since the process we use doesn't support inductor. Resistor still has some advantages. It save chip area and tend to operate over a broader bandwidth. Fig. 2.4 gives a double-balanced mixer with source degeneration.

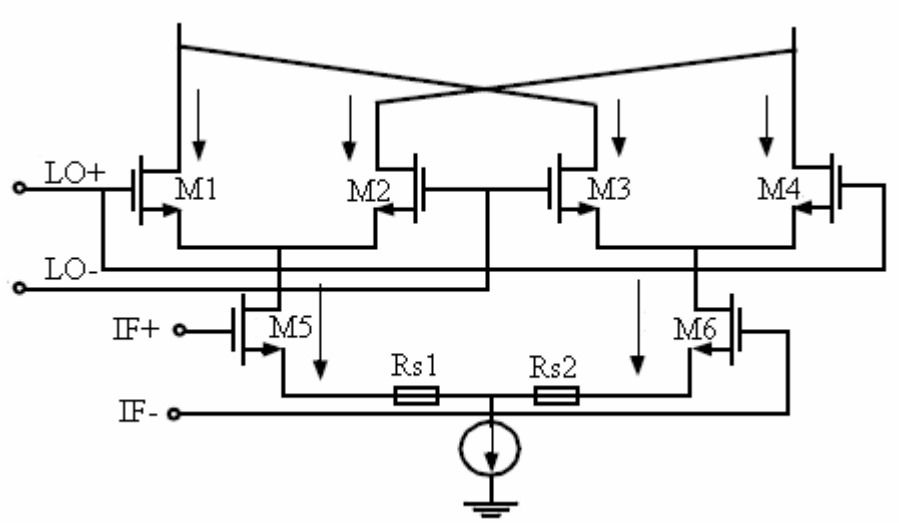

Fig. 2.4 Double-balanced Mixer with Source Degeneration

The gain of the mixer is given as following:

$$\frac{V_{RF}(t)}{V_{IF}(t)} \approx \frac{2}{\pi}\left(\frac{R_L}{R_s + \frac{1}{g_m}}\right)$$

2.4 Double-balanced Mixer Design.

In the analog circuit, transistors often operate in the saturation region, unlike the digital circuit with transistor working in triode region. Saturation region offers

higher gain and the current through transistors are less susceptible to the changing voltage across drain and source. Also when design analog circuits, first step is generally to specify biasing current and voltage [3] according to the design specification, then decide the transistor aspect ratio. This is the case for mixer design; a bunch of biasing networks is designed to bias transistors into saturation region. Fig. 2.5 gives the bias voltage assignments.

In the initial design, all the transistors length is chosen to be the minimum. The biasing current is chosen to be around 5mA. The source degeneration resistor is calculated to be 200Ohm.

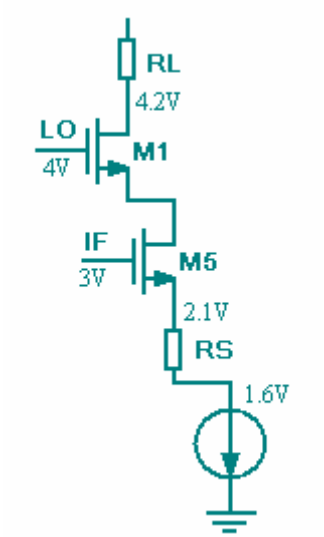

Fig. 2.5 Biasing Voltage Assignment

Current Sink Design:

Initially, I chose V_{GS} of M2 in current source around 1V, and its size ratio is chosen to be $W/L = 24/0.6$, The resistor R0 is 63.4k.

To generate about 5mA biasing current, the M1's size ratio is calculated as $W/L \approx 300/0.6$. The whole circuit of current source is given in Fig. 2.6. And its simulation results are given in Fig. 2.7 and 2.8.

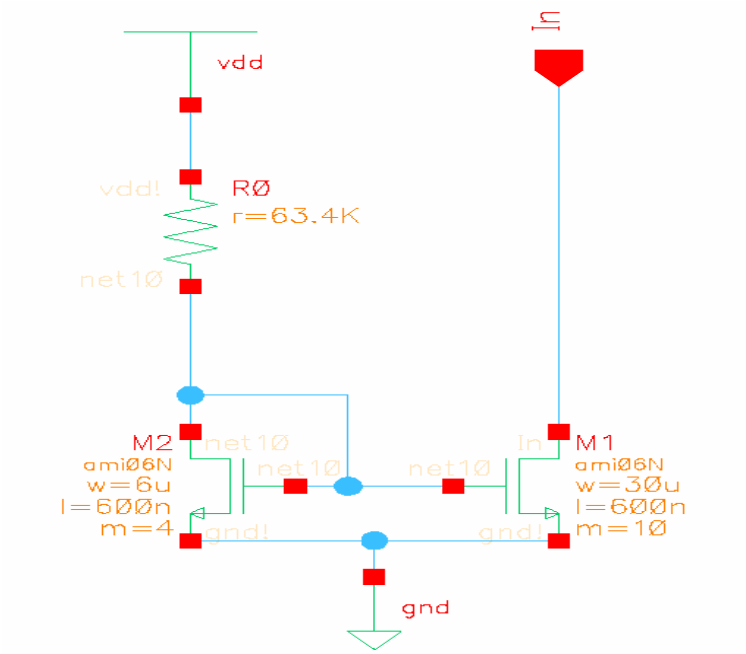

Fig. 2.6 Current Sink Schematic

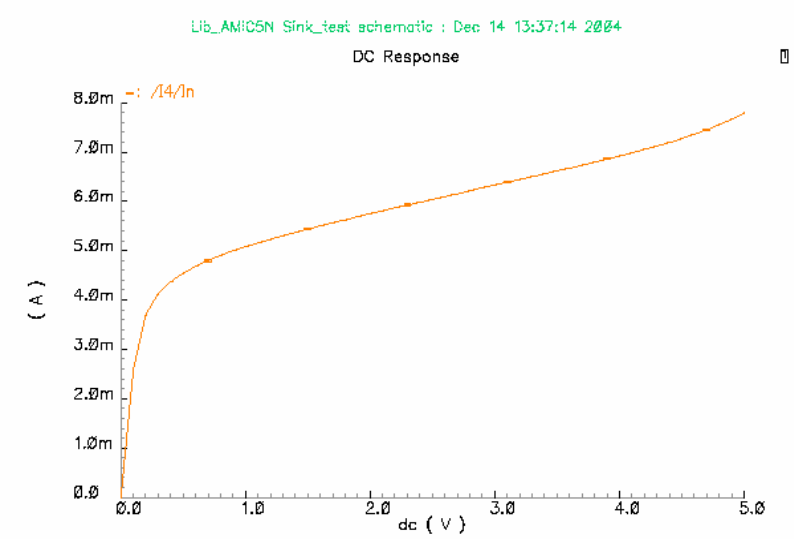

Fig. 2.7 DC Simulation of Current Sink.

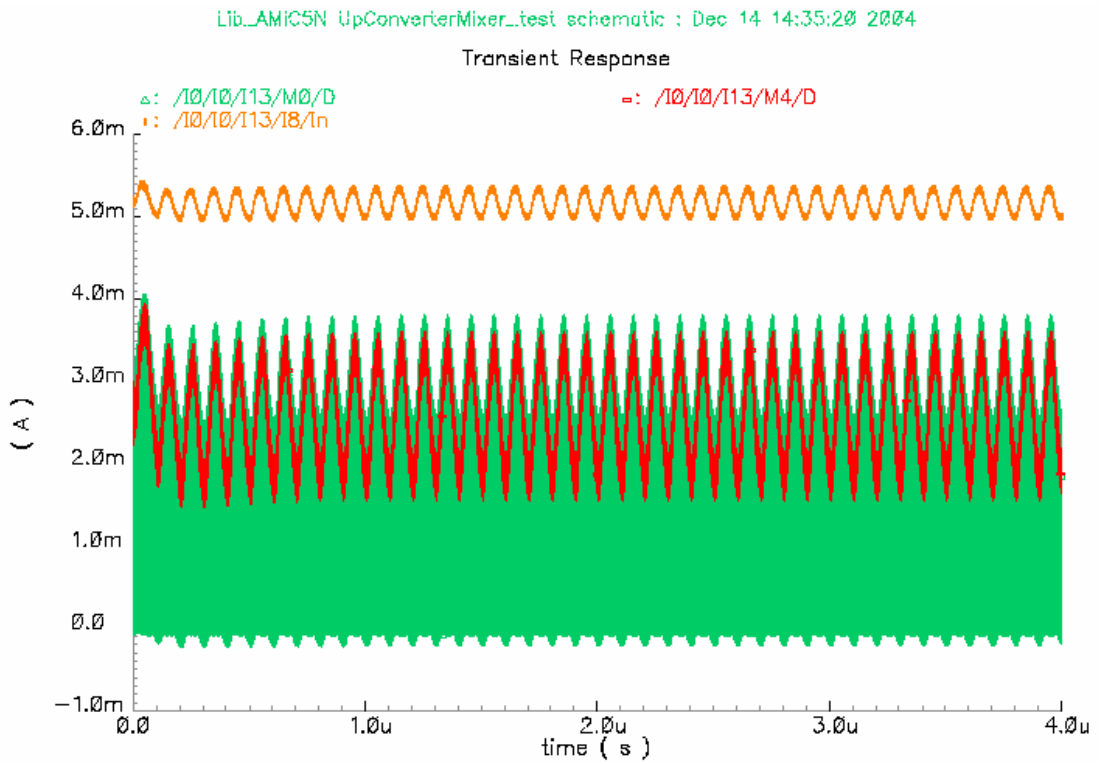

Fig. 2.8 Biasing Current.

The brown curve in the above figure is the biasing current value.

IF Input Transistor Sizing

When deciding the size of the IF input transistors, we should first specify the gain in the design specification. With specified gain, we can calculate the transconductance of those two transistors according to the following formula:

$$g_m \approx [\frac{2}{\pi}\frac{R_L}{Gain} - R_s] - 1$$

Then according to this g_m, the size ratio of the transistors are calculated according to:

$$W = \frac{g_m{}^2 L}{2K' I_{DS}}$$

In this project, I didn't take above design approach. The reason is that above design approach often involves SpectrRF design tools and corresponding RF model for analysis. The process AMIC5N is used in my design, and the RF model

is not provided. So, I calculated the size ratio by assuming that V_{GS} of the transistor is 1V with biasing current around 2.5mA, which resulting in $W/L = 150/0.6$ for IF input transistor.

LO Stage Transistor Sizing

For this stage, the transistor switching on and off, when they are on, they conduct 2.5mA current. The size is according to the following equation:

$$W = \frac{LI_{DS}}{K(V_{GS} - V_T)^2}$$

To make sure the transistor at LO stage operate in saturation region, a voltage around 4.2 V is chosen at the RF output. Then the load resistor is calculated as

$$R_L = \frac{VDD - V_{RF}}{i} \approx 300\Omega$$

By now we have decided the biasing condition for the mixer, but we still have not select the magnitude of the LO and IF input signals. LO signal is first considered. A noise contribution of the switching transistors arises from the interval of time in which both transistors conduct current and hence generate noise. Minimizing the simultaneous conduction interval reduces this degradation, so sufficient LO drive must be supplied to make the differential pair approximate ideal, infinitely fast switches. For this reason, LO signal is chosen to be square wave of certain magnitude. Of course, the lager the LO signal, the better the switching. But it can not be too big to make transistor out of saturation region. Also if LO signal is too large, a lot of current has to be moved into and out of the switching transistor during transitions. This can lead to spikes in the output signal, reducing switching speed and increasing LO feed-through. In this design, the LO signal is choose to be 0.8V.

IF signal also can not be very large to meet the saturation operation as well as feed-through requirement. The magnitude of IF signal in this design is chosen to be less than 1V.

By now, the mixer design is finished. The mixer still needs biasing network. This biasing network mainly consists of resistors and capacitors. Resistors are chosen to be large to reduce DC current. And the capacitors are chosen that its low end cut-off frequency is low enough to make the mixer be able to work under lower frequency, this is helpful in the testing stage.

The mixer circuit is given in Fig. 2.9, while mixer with biasing circuit is given in 2.10,

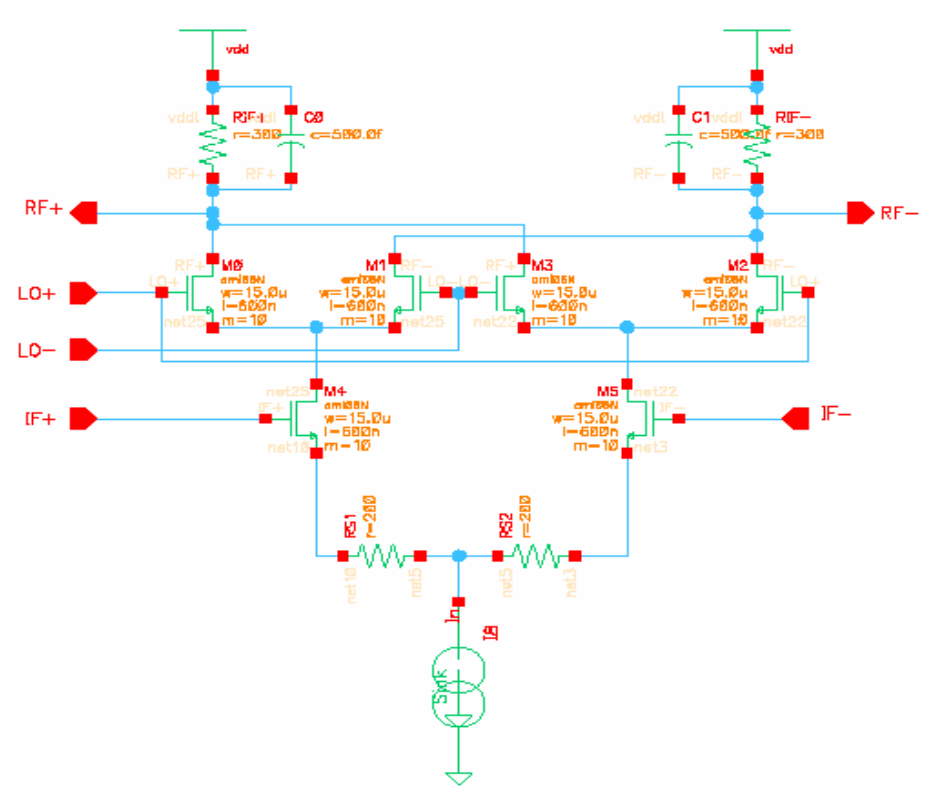

Fig. 2.9 Mixer Schematic

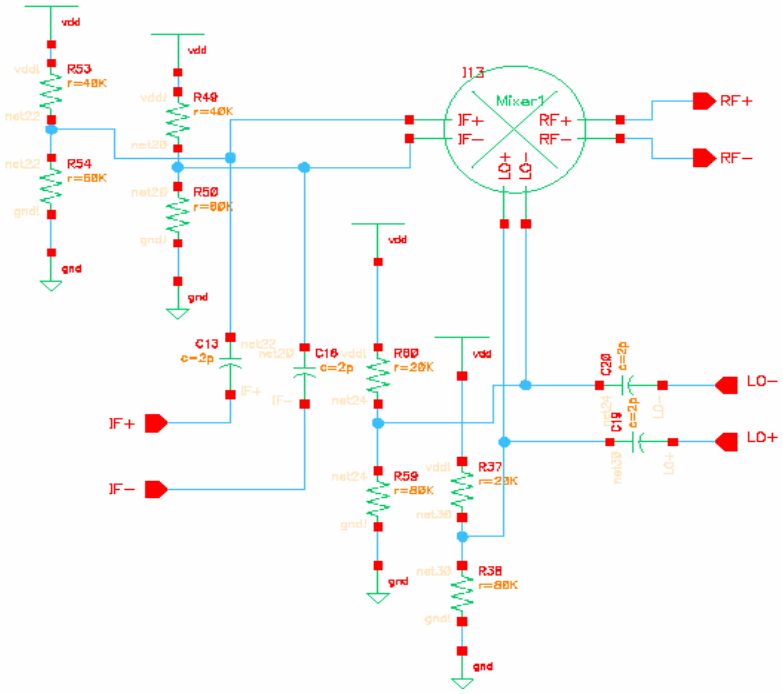

Fig. 2.10 Mixer_Biased Macro

The mixer's simulation results are given in the simulation section.

In Fig. 11 the current through one of the switching transistor is shown as green curve, we can find that the current through switching transistor is on and off, which has the effect of switching current from one output to the other.

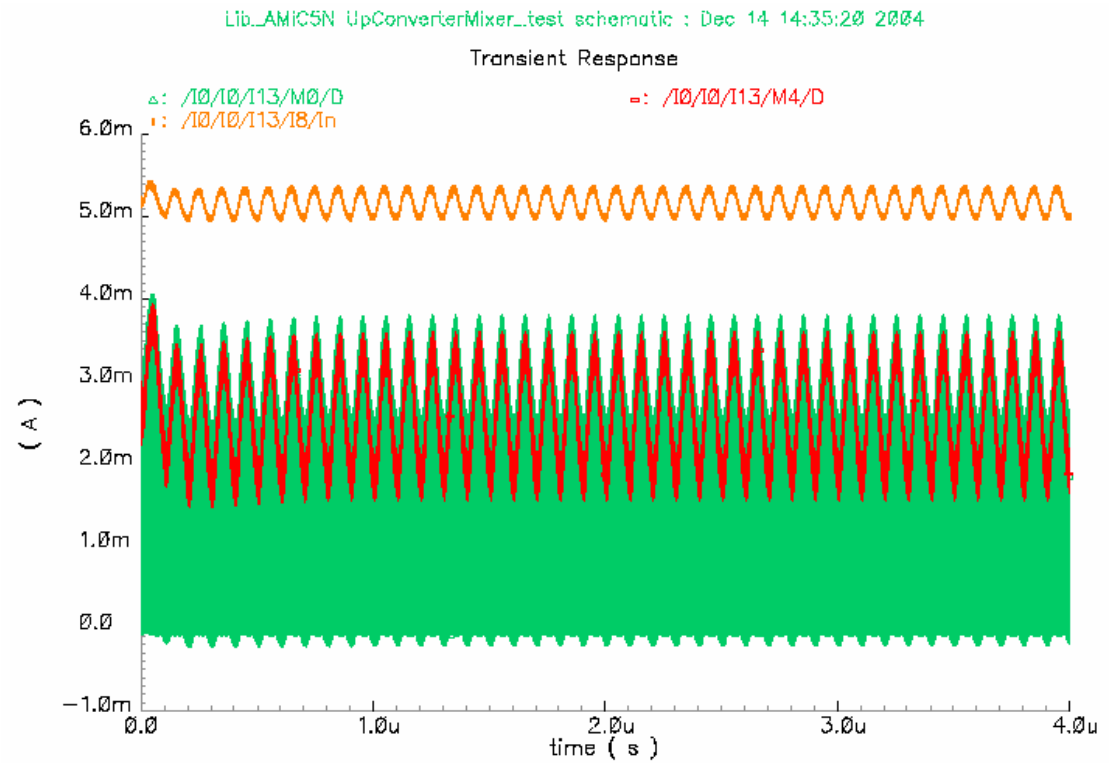

Fig. 2.11 Switching Stage Current

2.5 IF Signal Generation

There is 10MHz digital signal generated in the PLL block. From this signal, a small magnitude sine wave signal is generated by IF_Input block. This sine wave signal is used as the intermediate frequency to the mixer.

To generate sine wave from digital signal, three order of low pass filter is design like that in Fig. 2.12. Calculation according to the parameters, we found that the cut-off frequency is a little lower than 10MHz; this doesn't matter as long as a sine wave of desired magnitude is generated. The input 10MHz digital signal is buffered to the low pass filter; the buffering inverter can not be minimum size because the load effect of RC network can not be ignored. The output of the low pass filter is assumed to be small, so a current source load amplifier is followed to level it up. This 10MHz sine wave will drive the IF stage transistors plus biasing resistors network in the mixer, so a source follower is design to improve its driving ability. The whole schematic of IF_Input macro is given in Fig. 2. 12

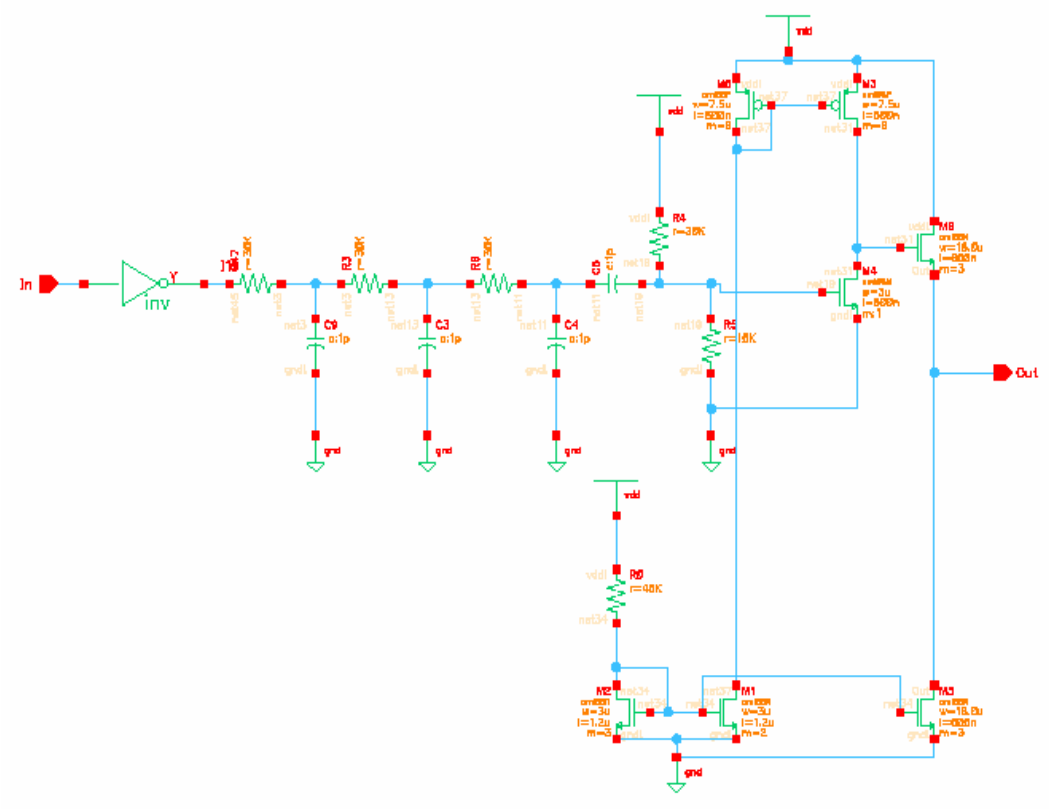

Fig. 2.12 IF_Input Macro Schematic

Fig. 2.13 shows the DC and AC simulations of the current source load amplifier used in this macro. From the DC figure we can find that gain is equal to 22.8dB. This amplifier's cut-off frequency is about 30MHz, which is high enough for this project.

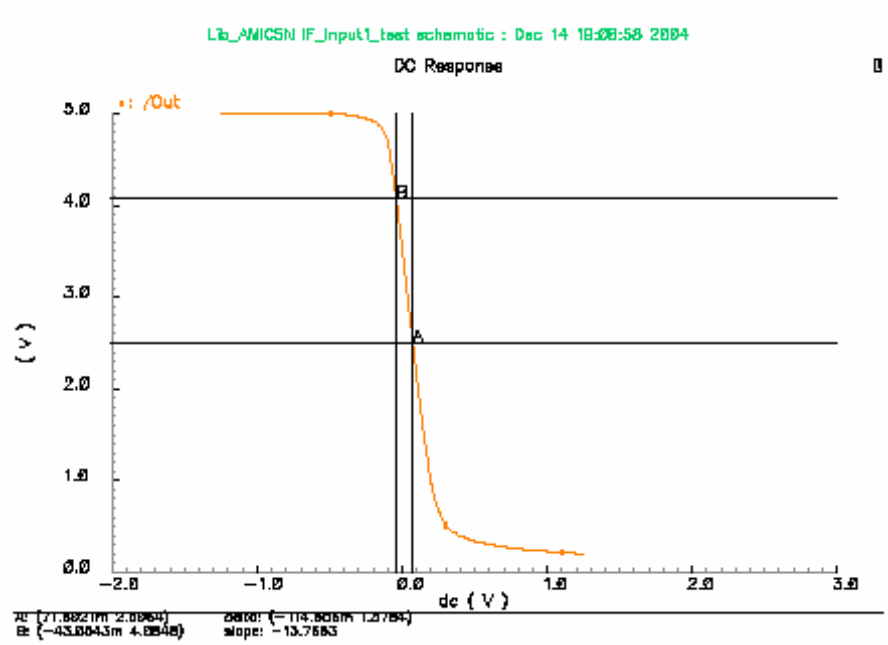

Fig. 2.13 DC Simulation of Current Source Amplifier

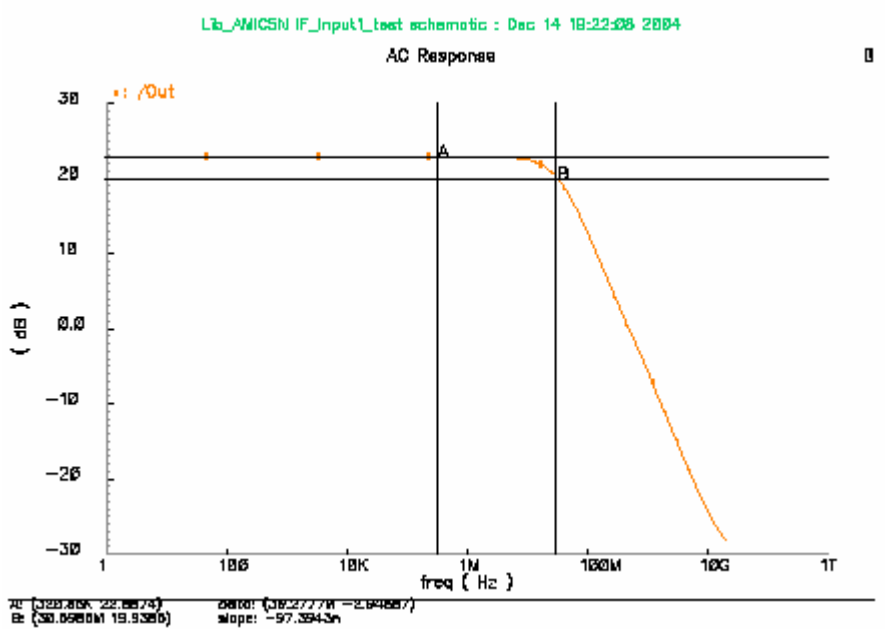

Fig. 2.14 AC Simulation of Current Source Amplifier

Fig. 2.15 shows the transient simulation of IF_Input macro. Its input is 5V digital input, through three order of low pass filter, much of harmonics are removed. This is displayed in Fig. 2.16.

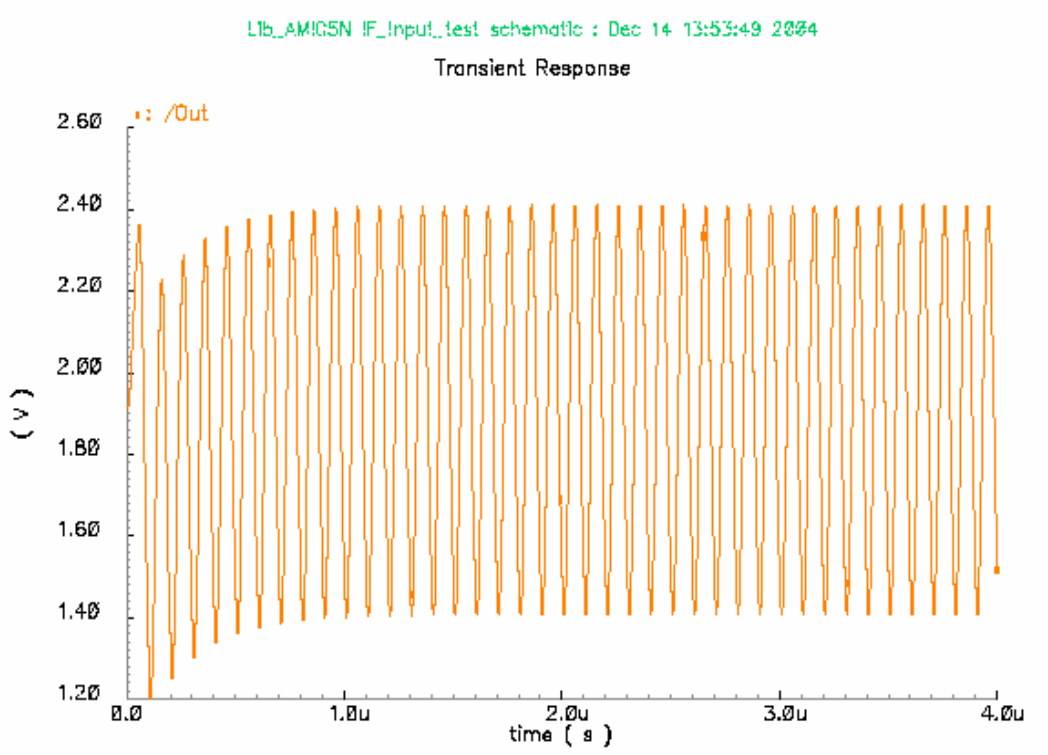

Fig. 2.15 Simulation Result

The Fig. 2.16 gives the Fourier Transform of the above output signal. The difference between desired signal and largest harmonic is 30dB, which is a good result.

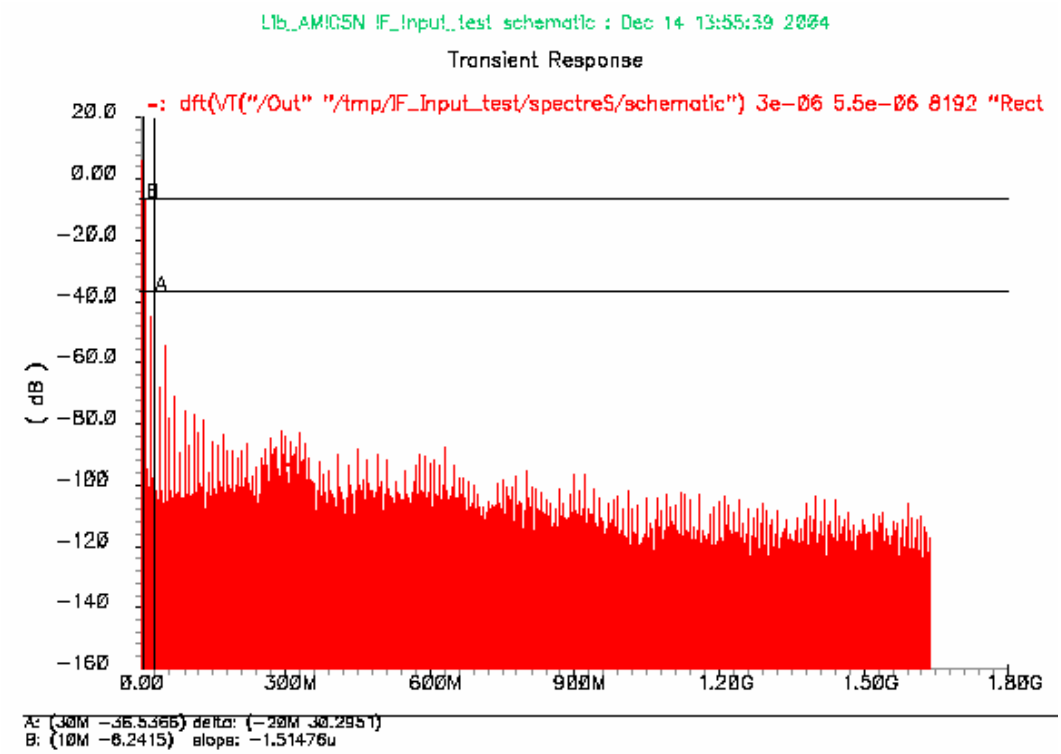

Fig. 2.16 Fourier Transform of the Output

2.6 Differential LO signal generation

The 320MHz signal from the PLL is of digital form. It can not be directly fed to the mixer. This signal has to be converted into differential signal of small magnitude. The most common way is to design a balun using inductor. But the process we use doesn't support inductor. So, some other way has to be found. A MOSFET with the same value resistors connected to its drain and source is shown in Fig. 2.17 [4]. Its small signal model has some symmetry. When a small signal applied to the gate, there are small signals of anti-phase at the output.

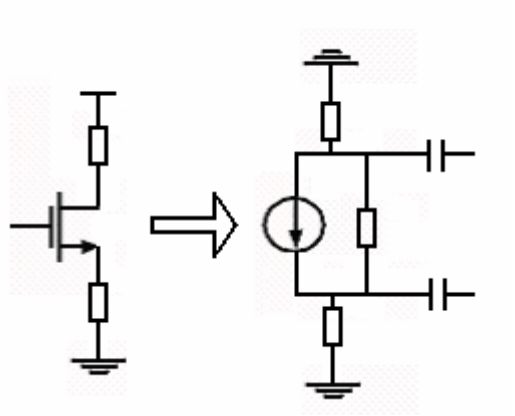

Fig. 2.17 Basic Concept of Differential LO Signal Generation

The single-ended input LO signal is a digital signal, this signal is divided into a small signal, and then ac coupled to the input transistor. The whole schematic of differential LO signal generation schematic is given in the Fig. 2.18.

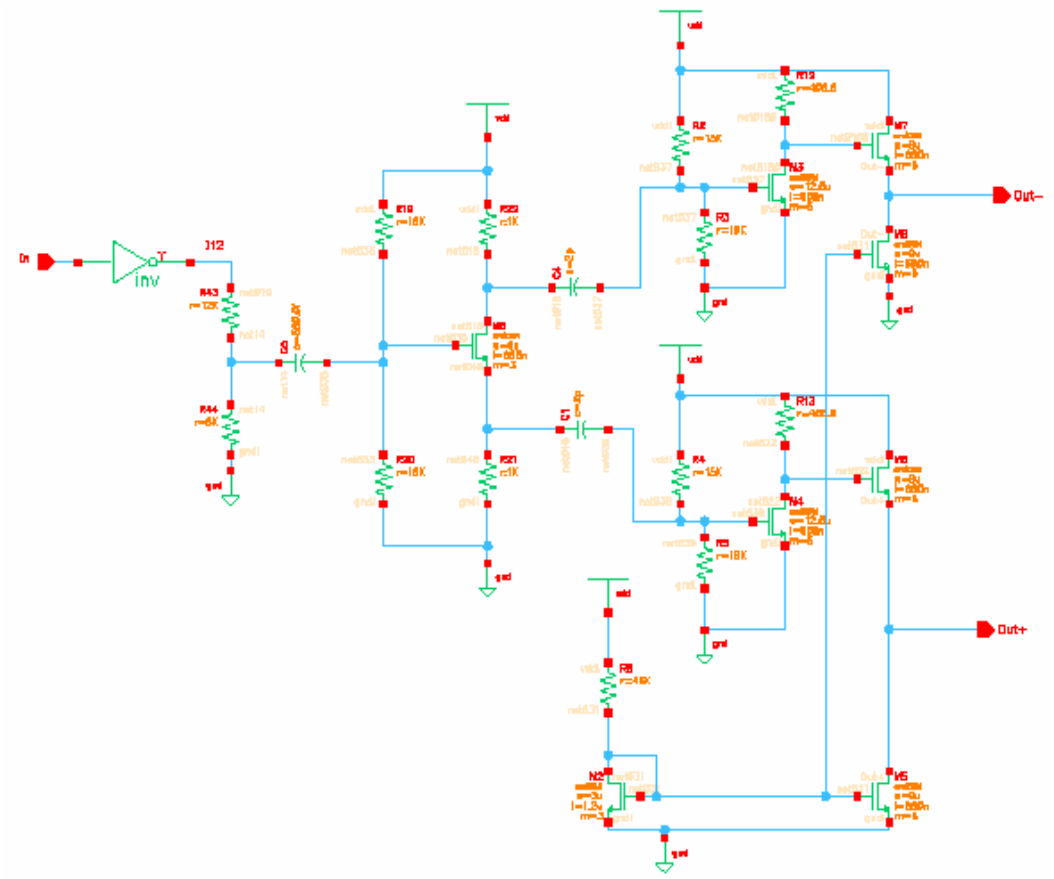

Fig. 2.18 Differential LO Signal Generation

There are two resistor-loaded amplifiers in the above circuit. They compensate for some signal loss of the single ended to differential stage. The resistor loaded

single transistor amplifier structure has small parasitic capacitance.

The two generated differential LO signals are fed to the switching transistor and biasing network in the mixer, those two switching transistors are of big size; therefore, the source follower is included in this stage to increase the signals' driving ability.

Fig. 2.19 gives the simulation results of LO signal generation stage, from the results we can find that differential signals are anti-phase and take the form of nearly square wave.

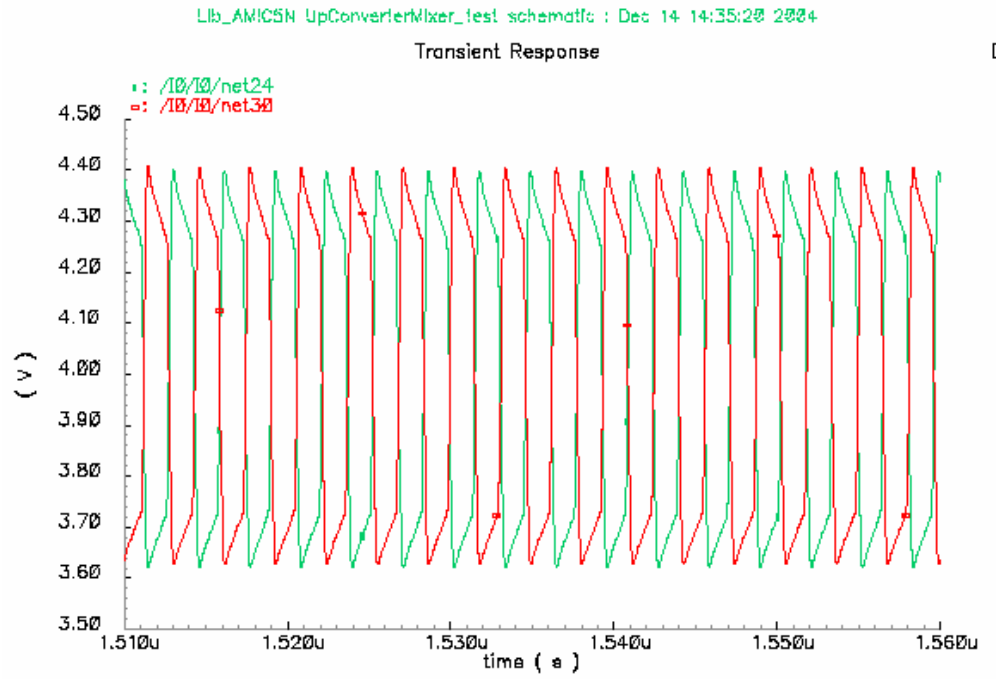

Fig 2.19 Transient Simulation of differential LO signal generation

Fig. 2.20 gives the bandwidth of the amplifier used in this stage. From this figure we can find that the amplifier's bandwidth is much higher than 320MHz.

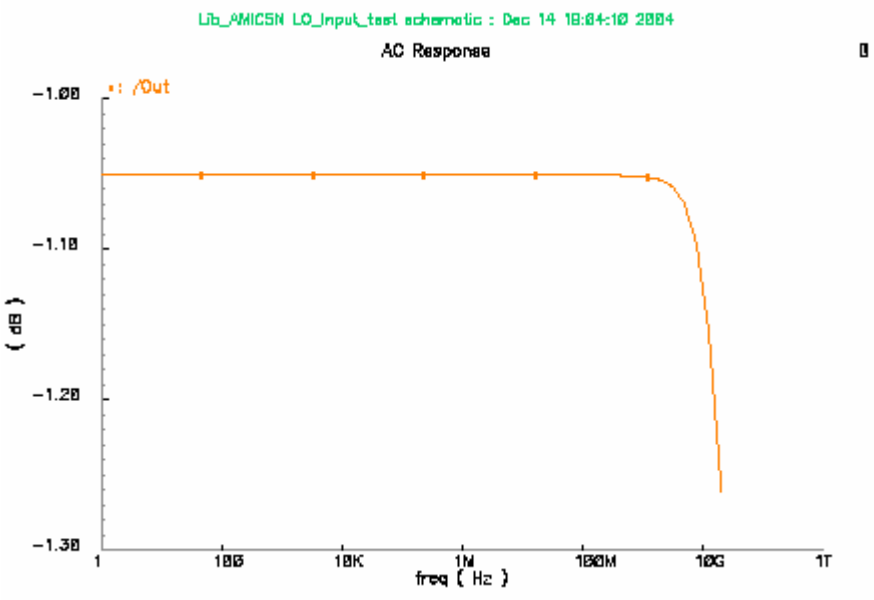

Fig. 2.20 AC Simulation of the Amplifier

2.7 Diff-to-Single Macro Design

The diff-to-single block provides amplification and differential to single ended signal conversion. The outputs of mixer are two differential RF signals. Generally, those two signals will be converted into single ended signal and fed to the following filter. In my design, some simplification is taken and the above filter is not designed. After the differential signals are converted into single one, it is fed into a modulator.

The differential-to-single converter consists of a differential pair with resistor loads. The output is taken from one side as the single-ended signal. The resistor load has the advantage of not introducing two much parasitic capacitance, therefore it has very large bandwidth. The Diff-to-Single block with biasing network is shown in the Fig. 2.21.

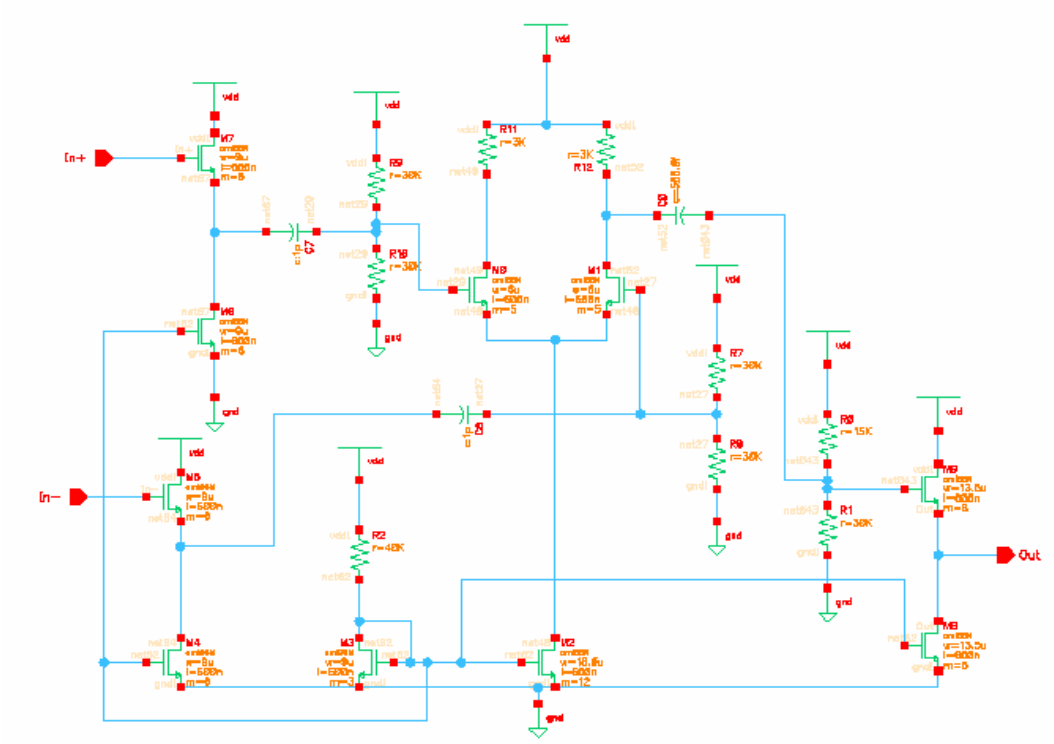

Fig. 2.21 Diff-to-Single Macro

The DC and AC simulation of differential pair without biasing network is done and the results are given in Fig. 2.22 and Fig. 2.23. Its gain is about 6dB and bandwidth is larger than 320MHz. Figure 2.24 shows the transient simulation results.

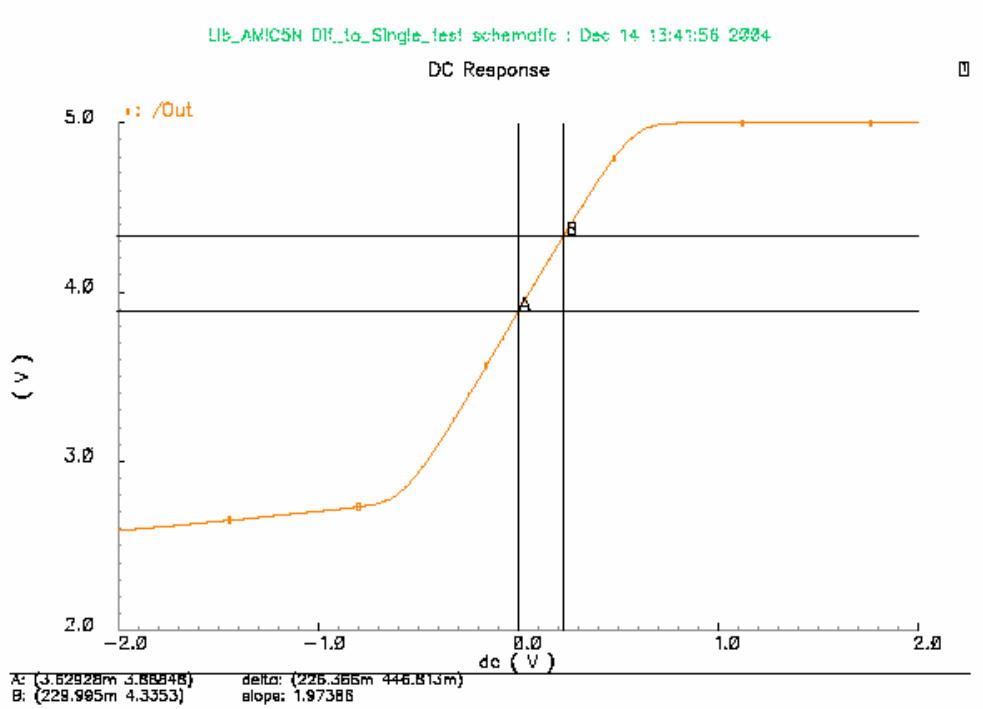

Fig.2.22 DC Simulation of Differential Pair

From the Fig. 2.22, we can find that the linear region for the diff pair is from about -0.5V to 0.5V.

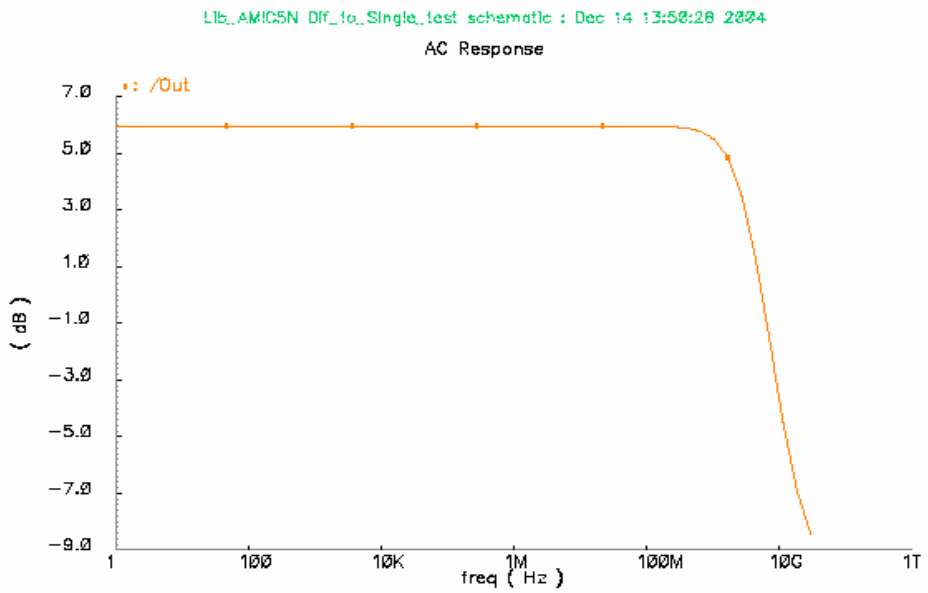

Fig. 2.23 AC Simulation of Differential Pair

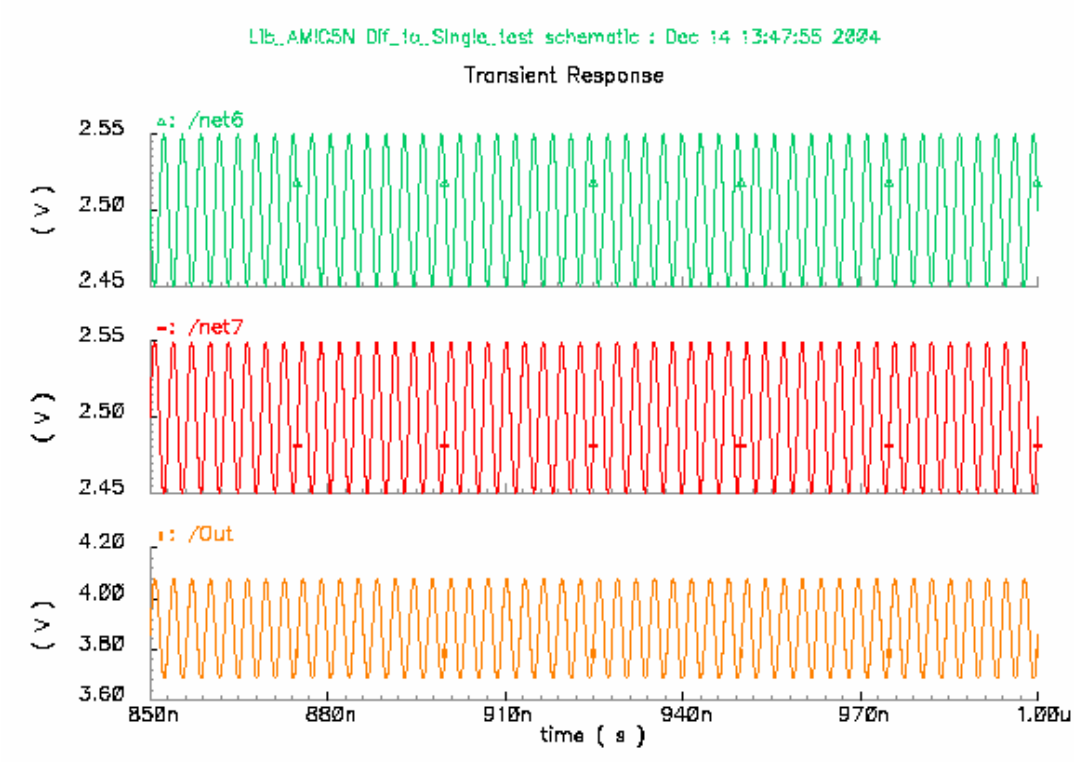

Fig. 2.24 Transient simulation of Diff_to_Single Macro

As for this differential pair design, we should pay attention to the distortion. The input to this stage should be within its linear region. If not, we should adjust the biasing current. The following equation can give some intuition about how to change the difference between the differential signals [5].

$$|V_{id}| \le \sqrt{2}\left(\sqrt{\frac{2I_{d1}}{k'(W/L)}}\right)|_{V_{id}=0} = \sqrt{2}(V_{ov})|_{V_{id}=0}$$

V_{id} is the difference between the two differential signals. From this equation, we can find that the range of V_{id} for which both transistors operated in saturation region is proportional to the overdrive calculated when $V_{id} = 0$. This range of differential pair can be adjusted by changing the value of the source current and the aspect ratio of the input transistors. In my design, I changed the biasing current.

2.8 LO_Input Macro design

In this design, FSK modulation scheme is adopted. The output is switching between 320MHz carrier signal and the 330MHz output of mixer. This 320MHz

should be sine wave signals. It is generated in the similar way as the generation of IF signal. Here two-order low pass filter is designed. If all parameters are calculated rigorously to design the filter with –3dB bandwidth of 320MHz, then at the 320MHz point, the slope is less than 40dB/dec. So, the cutoff frequency is design to be a little small than the 320MHz. Similar to that in IF stage, the buffering inverter for the input signal cannot be minimum size to drive the low pass filter. The output signal of the filter is expected to be small, so an amplifier with resistor load is designed. This amplifier with resistor load has larger bandwidth shown before. The voltage gain is give as follows:

$$A_v = \frac{v_o}{v_i} = -g_m(r_o \parallel R_D)$$

The output signal is driven by a source follower to the next stage. Without this follower, the signal will experience an obvious load effect. The Fig. 2.25 gives the schematic of LO_Input macro. The spectrum of the output of this stage is given in Fig. 2.26. The difference between desired signal and its second order harmonic is about 45dB.

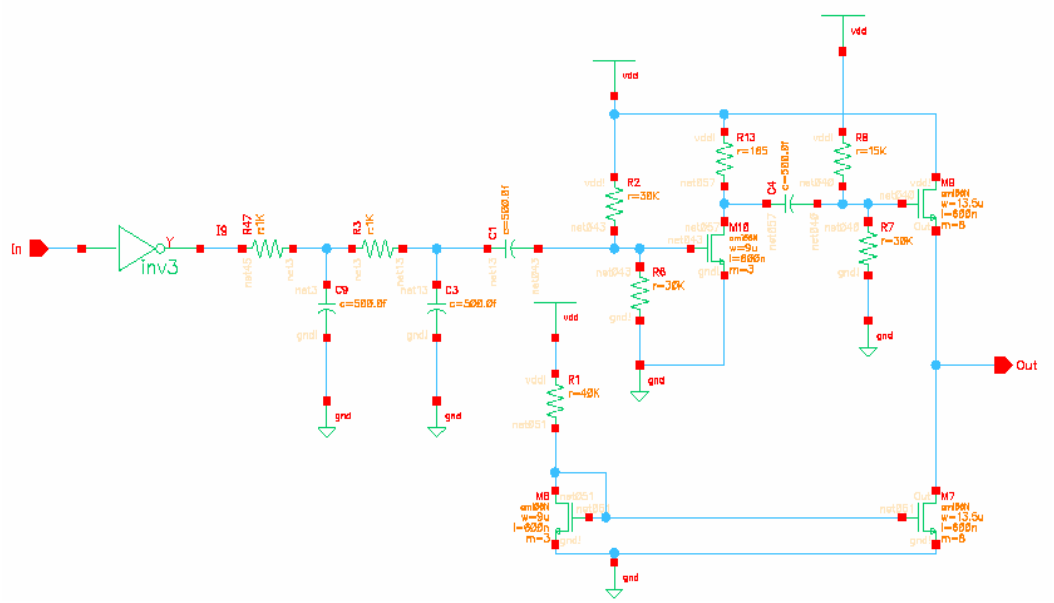

Fig. 2.25 LO_Input Macro

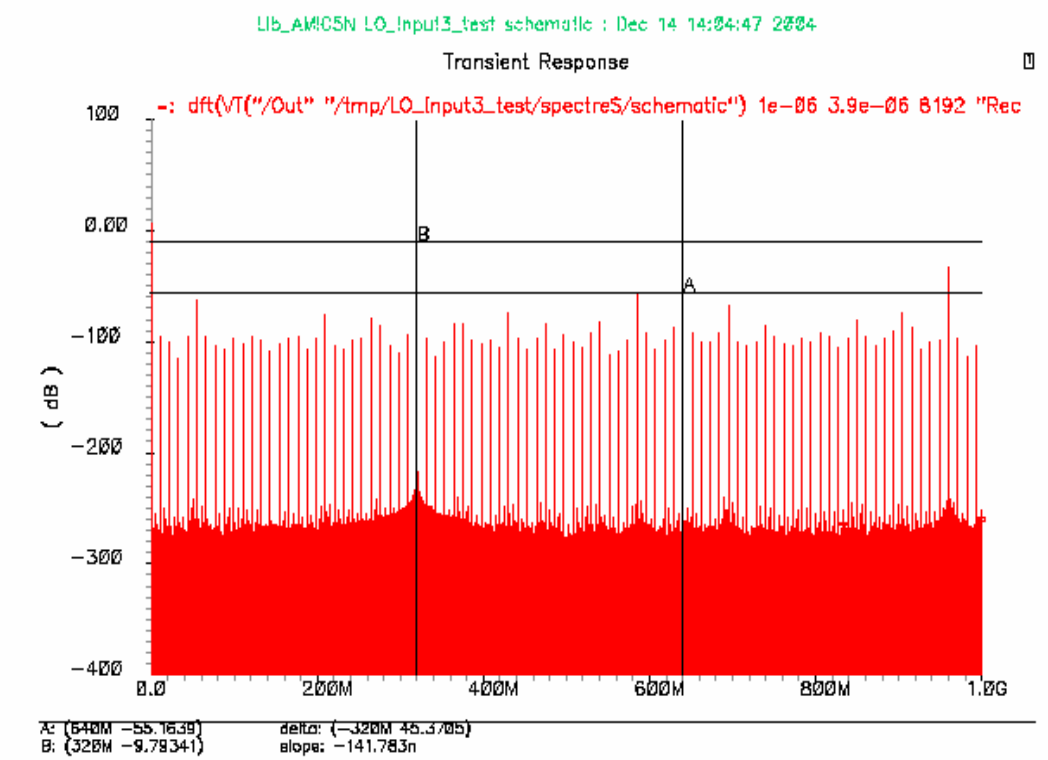

Fig.2.26 Spectrum of LO_Input Macro Output

In the Diff-to-Single and LO_Input macros, source followers are used. Those two source followers can be used as level shifter for the output as well as buffer. The output DC voltages are fixed at the same point. So for the parasitic capacitance of the late stage, there is no large signal charging and discharging. The difference between the voltage level of the input gate and output source can be specified by controlling W/L ratio according to the following equation.

$$V_{GS} = V_{in} - V_o = V_{TO} + \gamma(\sqrt{\phi + V_O} - \sqrt{\phi}) + \sqrt{\frac{2I_{DS}}{\beta}}$$

2.9 Modulator Design

In this modulator the FSK scheme is implemented. The bit sequence generated in Sequence Generator stage is used to switch the two signals to the analog buffer. This analog buffer is designed based on the previous design. It can drive a large capacitance still have a wide –3dB bandwidth. Its DC and AC simulation results are given in Fig. 2.28 and Fig. 2.29.

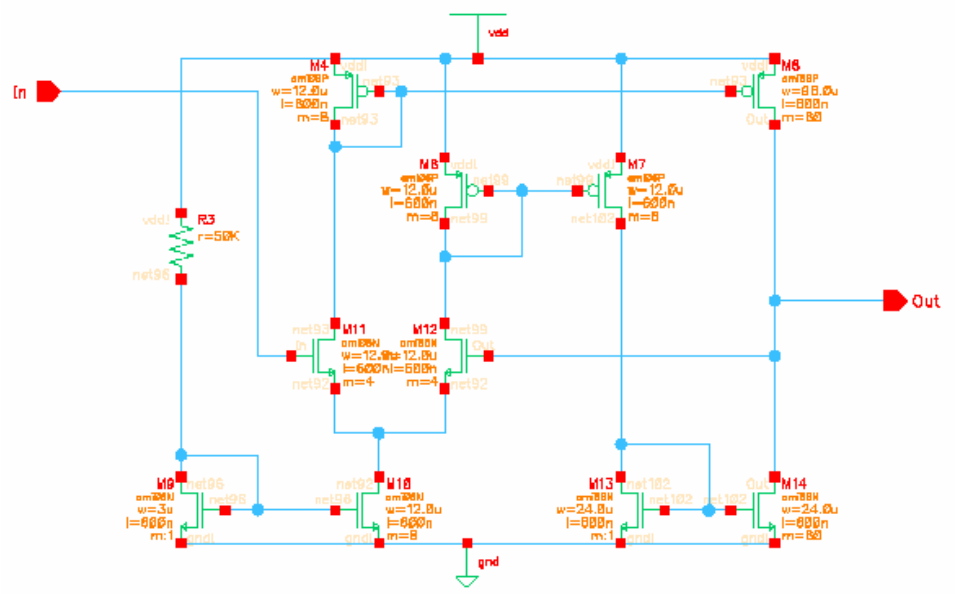

Fig. 2.27 Analog Buffer

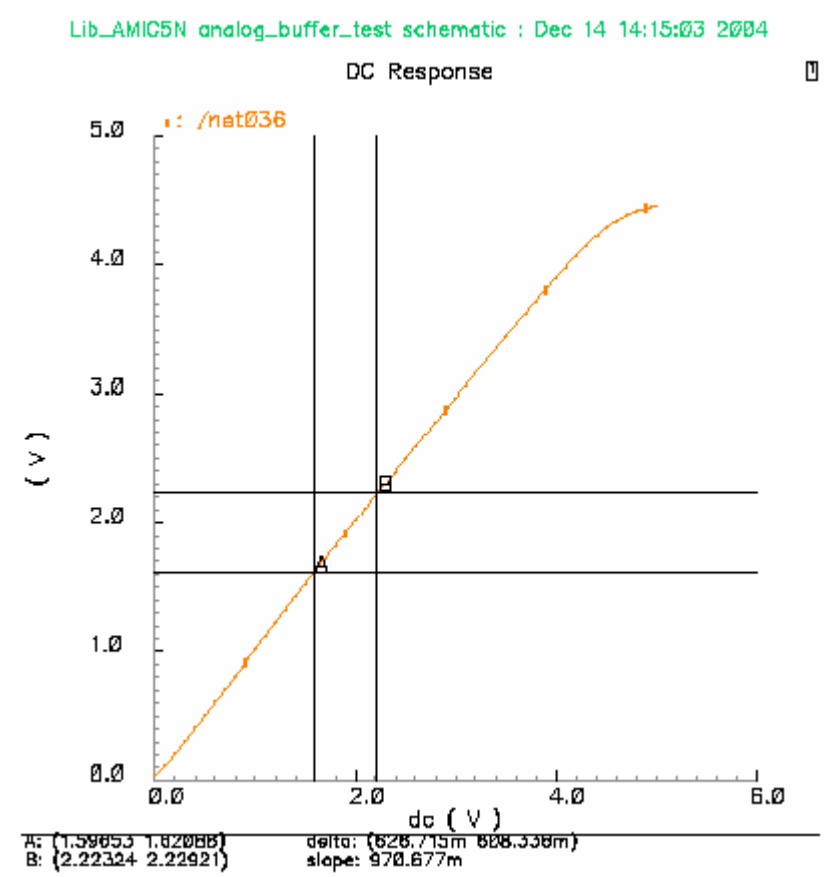

Fig. 2.28 DC Simulation of Analog Buffer

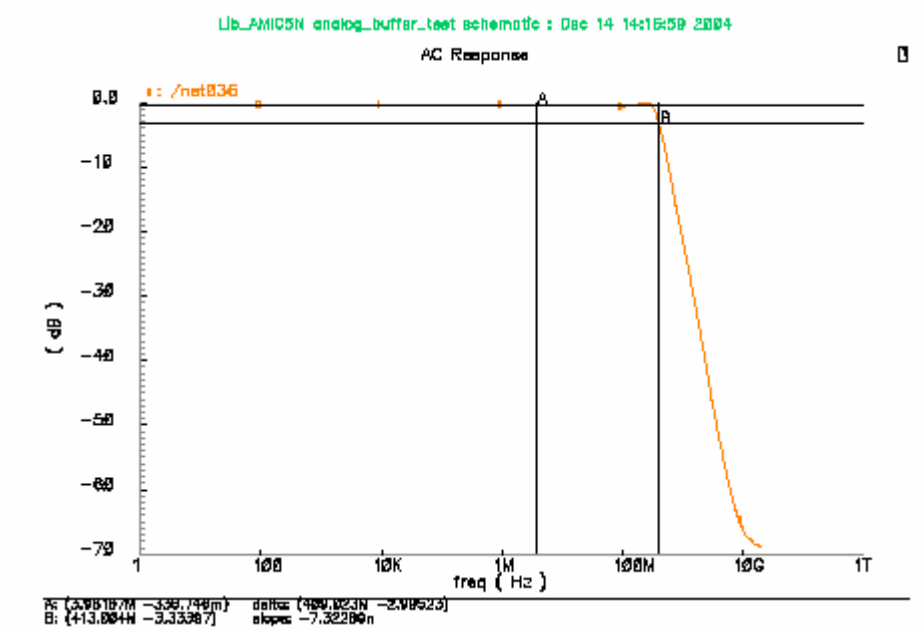

Fig. 2.29 AC Simulation of Analog Buffer

Fig. 2.30 displays how the FSK is implemented in this design. Two NMOS are used as switches. As I mentioned previously, the DC voltage at the input of analog buffer is fixed because of level shifts in the previous stages. This prevents the charging and discharging of the parasitic capacitance of the input transistor in the analog buffer, which help to remove the spike that could otherwise appears at the output signal.

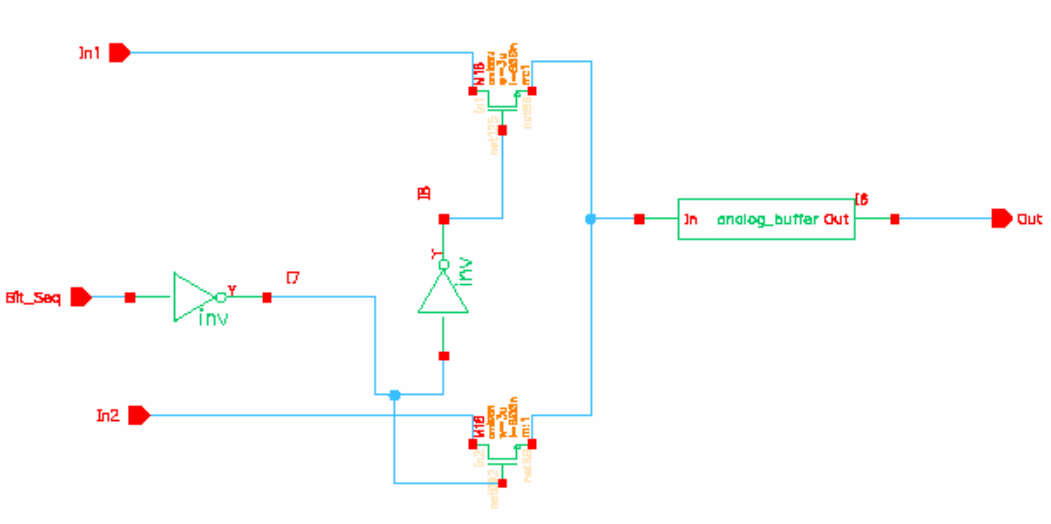

Fig. 2.30 Modulator Schematic

3 Simulation

3.1 The Top Level Simulation Results

We first do the simulation of mixer with digital input signals. The schematic is given in the Fig. 3.1

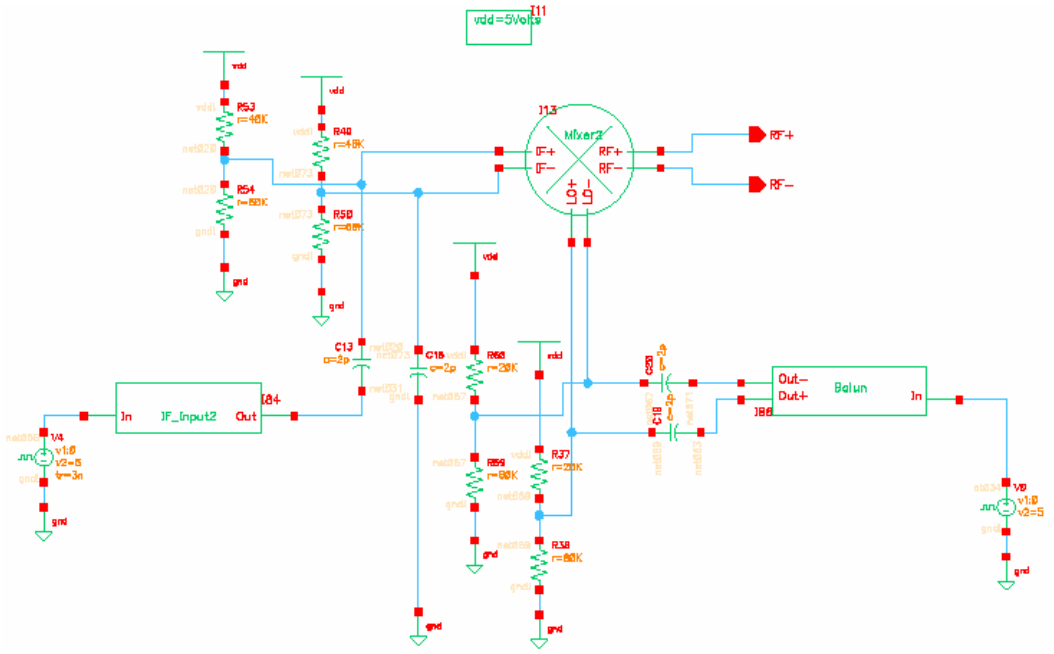

Fig. 3.1 Top Level Simulation

In the Fig. 3.2, the current values are plotted. The green curve is the current flow through the LO switching transistor. It keeps turning on and off. The red curve is the current passing through the gain stage transistor in the mixer. The brown line is the biasing current. From the figure, we can find that LO and IF signals are coupled into biasing current. The reason is that in this design, the simple current source is used, which is sensitive the drain-source voltage change. Other structure of current source can be used to improve its performance. Ac grounding the gate of transistor in the current source is a good practice.

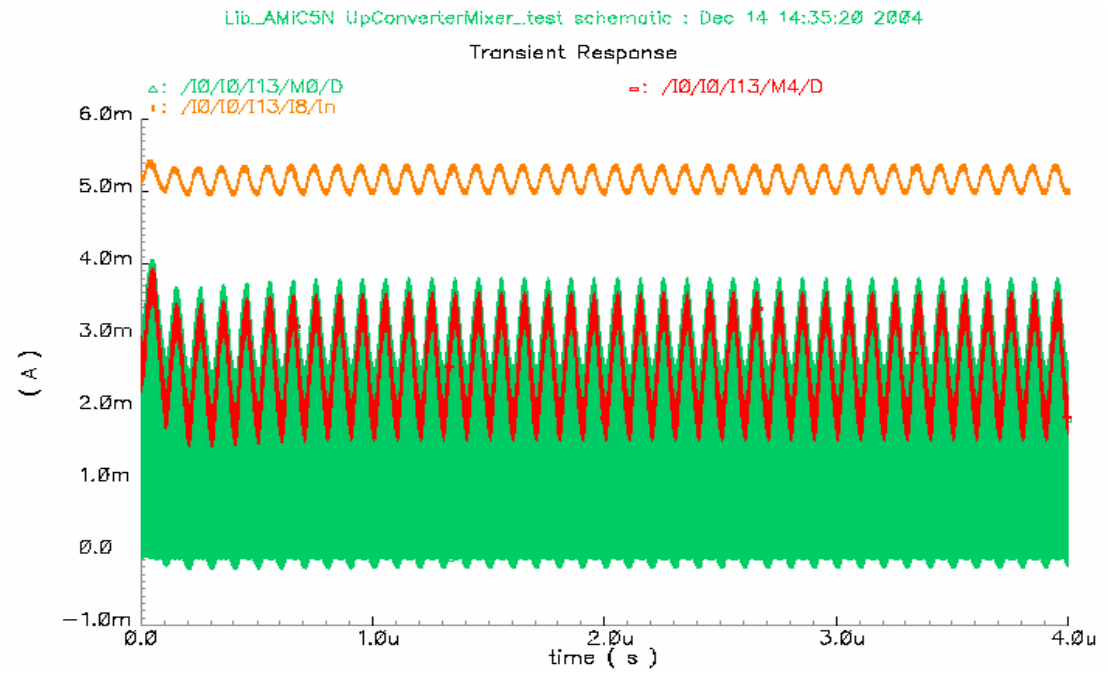

Fig. 3.2 Current Value in the Mixer

In the mixer, IF+ input is fed by the signal generated by IF_Input block, which is shown as brown curve in the Fig. 3.3. IF- input in the mixer is ac grounded; its voltage is shown to be 3V DC voltage.

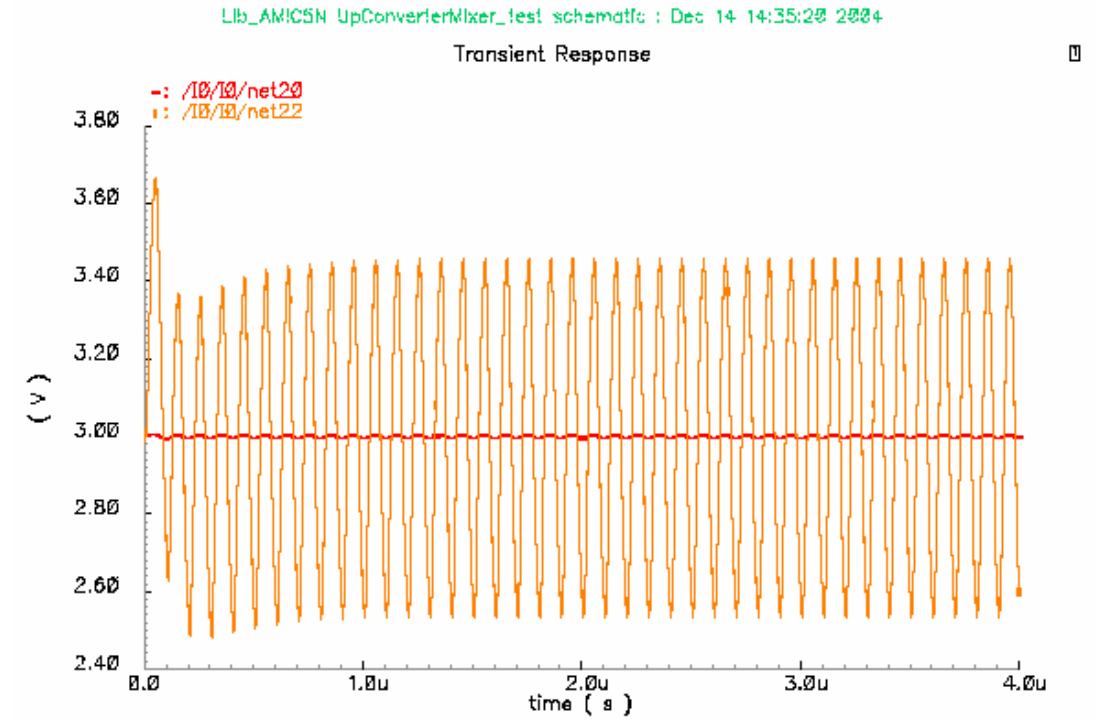

Fig. 3.3 IF+ and IF- Input Signals

The following two figures shows the LO signals appear at the mixer's LO+ and LO- port. We can find that the two signals have anti-phase property from Fig. 3.5.

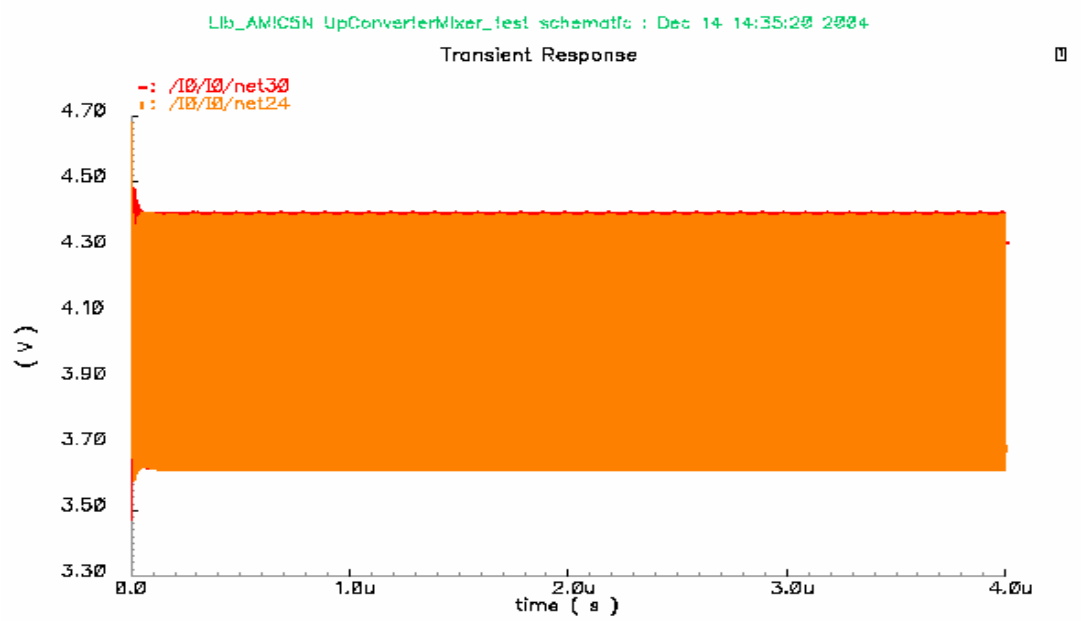

Fig. 3.4 LO+ and LO- Input Signals

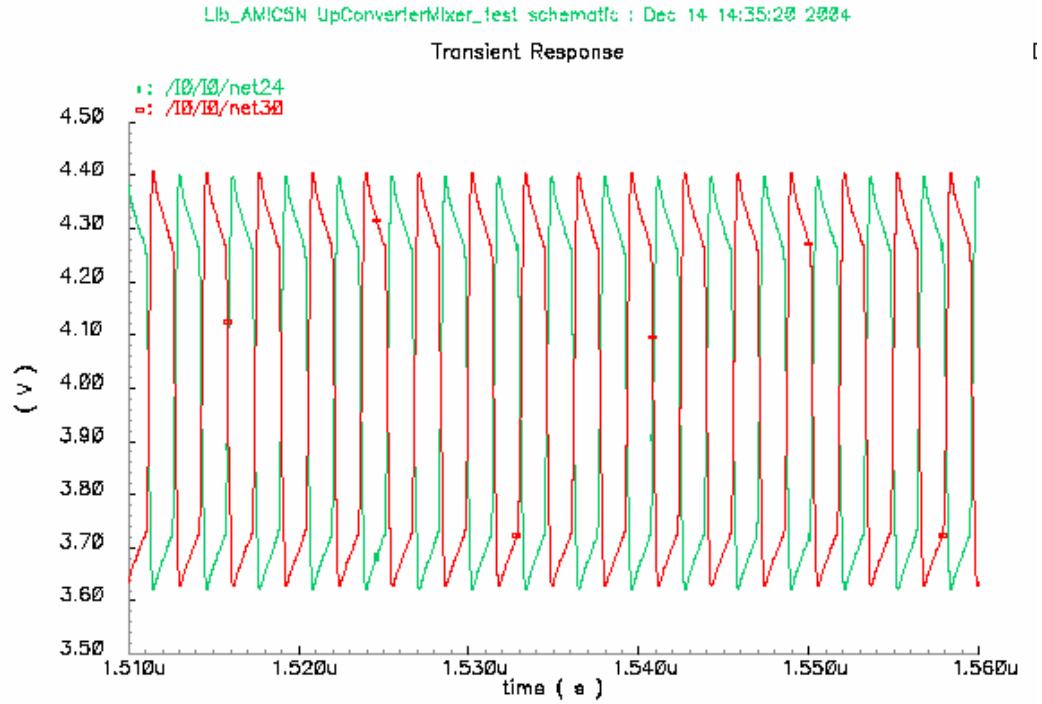

Fig. 3.5 LO+ and LO- Input Signals

The mixer's differential outputs are shown in Fig. 3.6. The peak-to-peak values for both signals are within 0.5V, so there is no distortion problem when fed to the Dif_to_Single block.

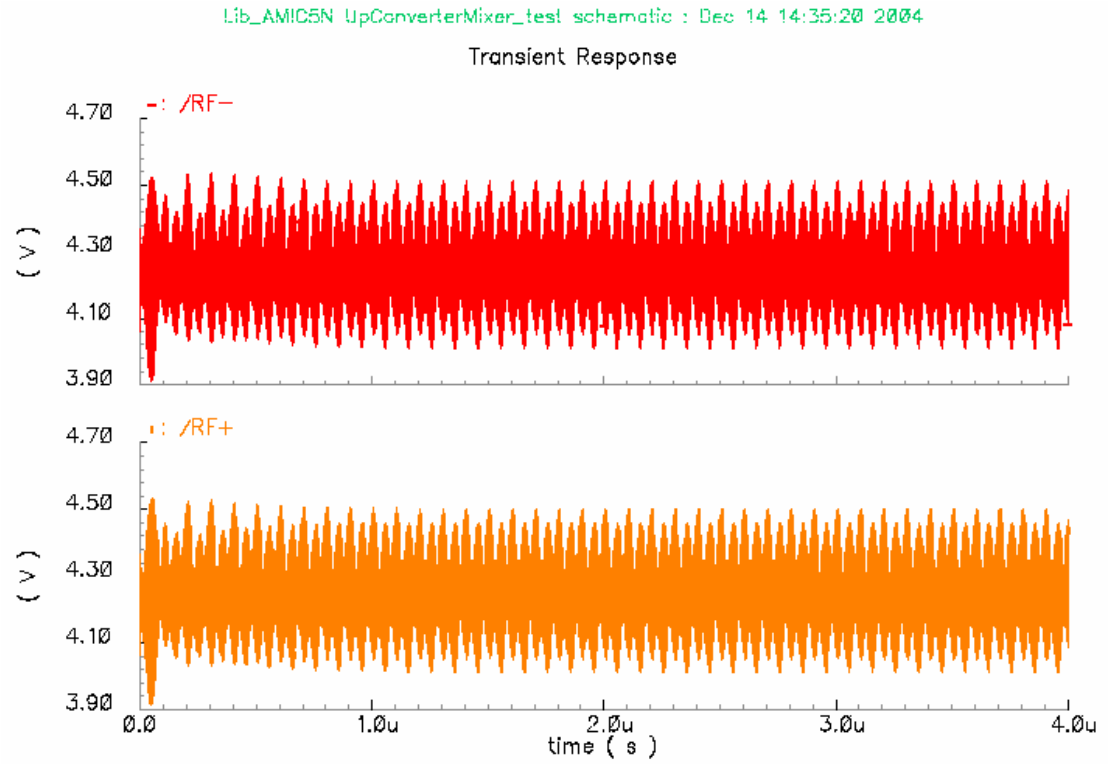

Fig. 3.6 Differential Output of the Mixer

4 Physical Design

The general design rules are followed for all layouts. The routing width is determined by the magnitude of current flow through the path, one micrometer per milliamp. The analog buffer consumes about 100mA current, so the VDD and GND bus for this buffer is at least 100um. Most of the components in a block have guard rings around. This will reduce noise from the neighboring component or block. The large MOSFETs are laid out with multiplier to reduce the parasitic capacitance. Those concerns are shown in the following example layout.

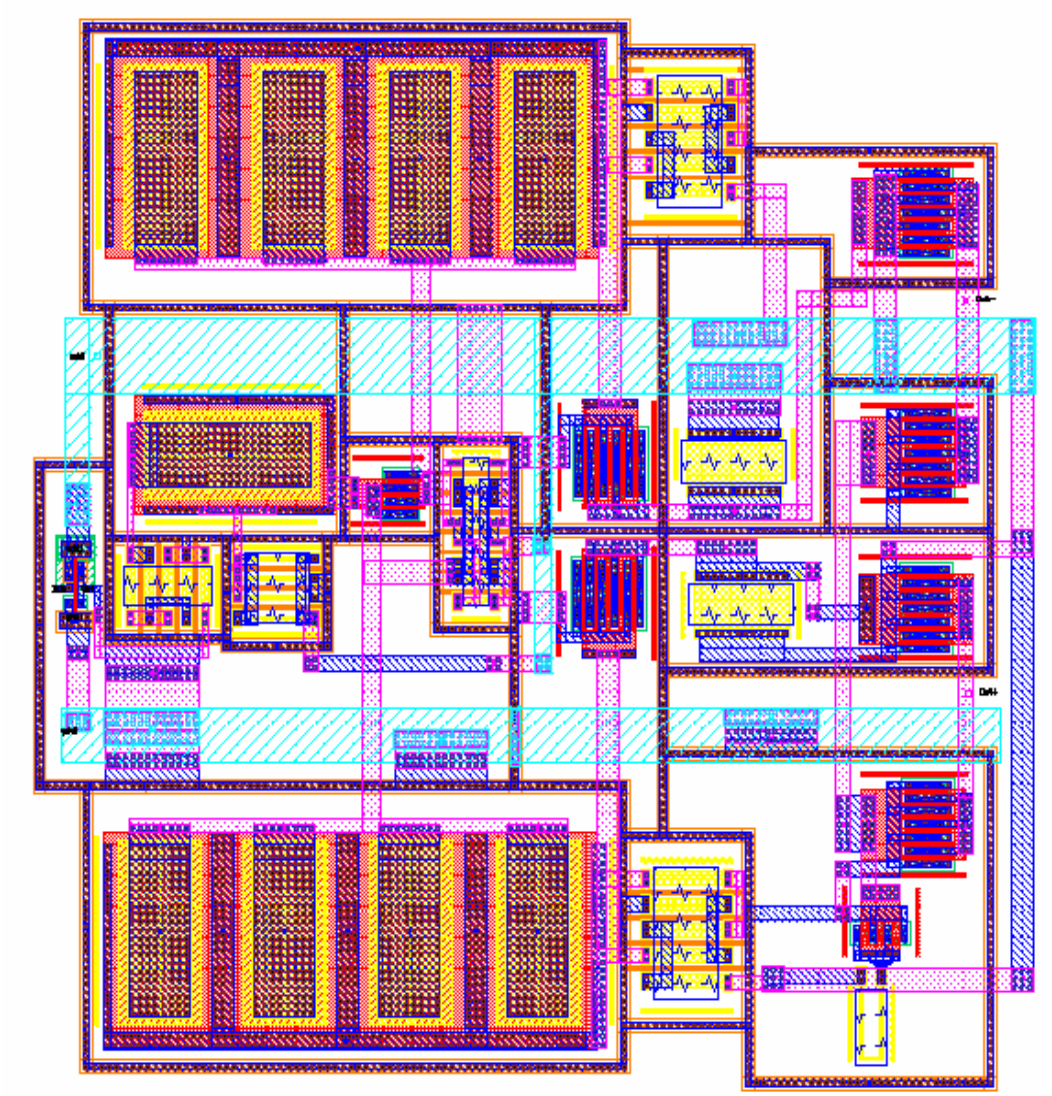

Fig. 4.1 Single-to_Differential Converter Layout

In the above layout example, the antenna rule is applied. The unit cell concept is applied in resistors and capacitances layout for good matching.

5 Verification

5.1 DRC and LVS Verification

This design passes all the DRC and LVS check. The LVS check is also made between final GDSII file and original schematic, and its LVS output file is given as following:

@(#)$CDS: LVS version 4.4.6 06/24/2003 17:52 (cds11607) $
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.

Net-list summary for /usr/grads/zzhu/ECE_547/AMIC5N/LVS/layout/netlist count

166	nets
0	terminals
150	res
67	cap
321	pmos
723	nmos

Net-list summary for /usr/grads/zzhu/ECE_547/AMIC5N/LVS/schematic/netlist count

97	nets
37	terminals
73	res
29	cap
26	pmos
83	nmos

2 net-list ambiguities were resolved by random selection.

The net-lists match.

layout	schematic	
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	1261	211
total	1261	211
	nets	
un-matched	0	0
merged	0	0

pruned	0	0
active	166	97
total	166	97

	terminals	
un-matched	0	0
matched but different type	0	0
total	0	37

Probe files from /usr/grads/zzhu/ECE_547/AMIC5N/LVS/schematic
devbad.out:
netbad.out:
mergenet.out:
termbad.out:
prunenet.out:
prunedev.out:
audit.out:

Probe files from /usr/grads/zzhu/ECE_547/AMIC5N/LVS/layout
devbad.out:
netbad.out:
mergenet.out:
termbad.out:
prunenet.out:
prunedev.out:
audit.out:

5.2 Extracted View Simulation

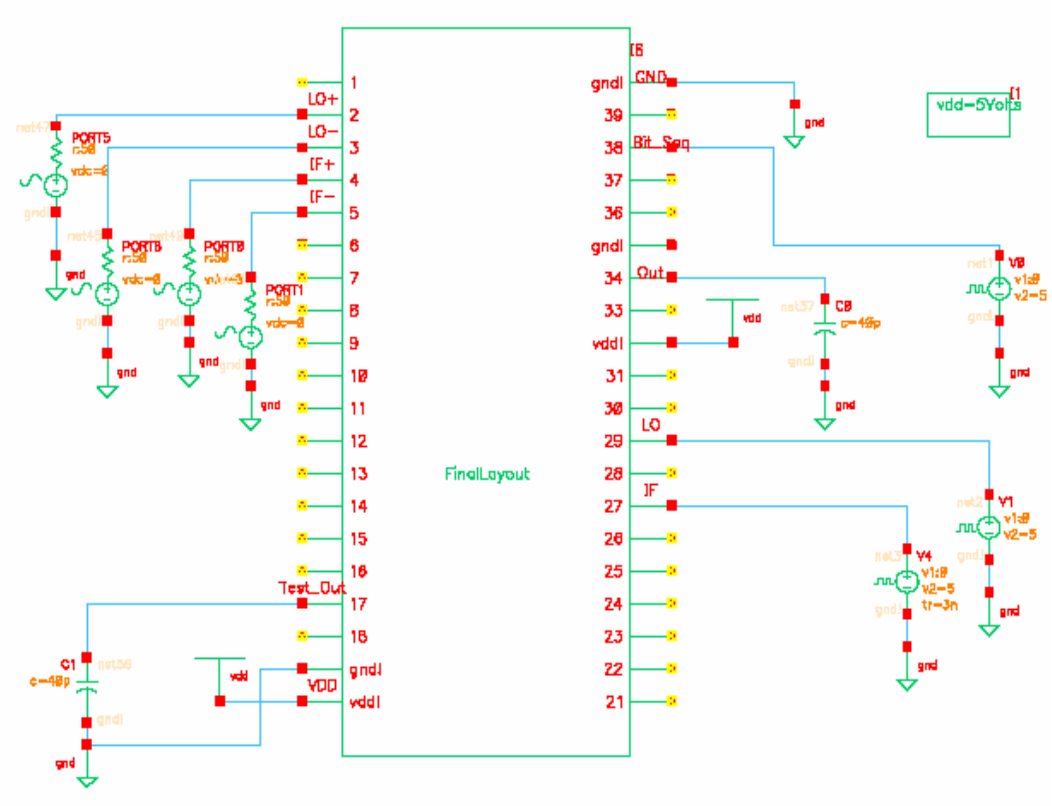

Fig. 5.1 Top Level Testing Circuit

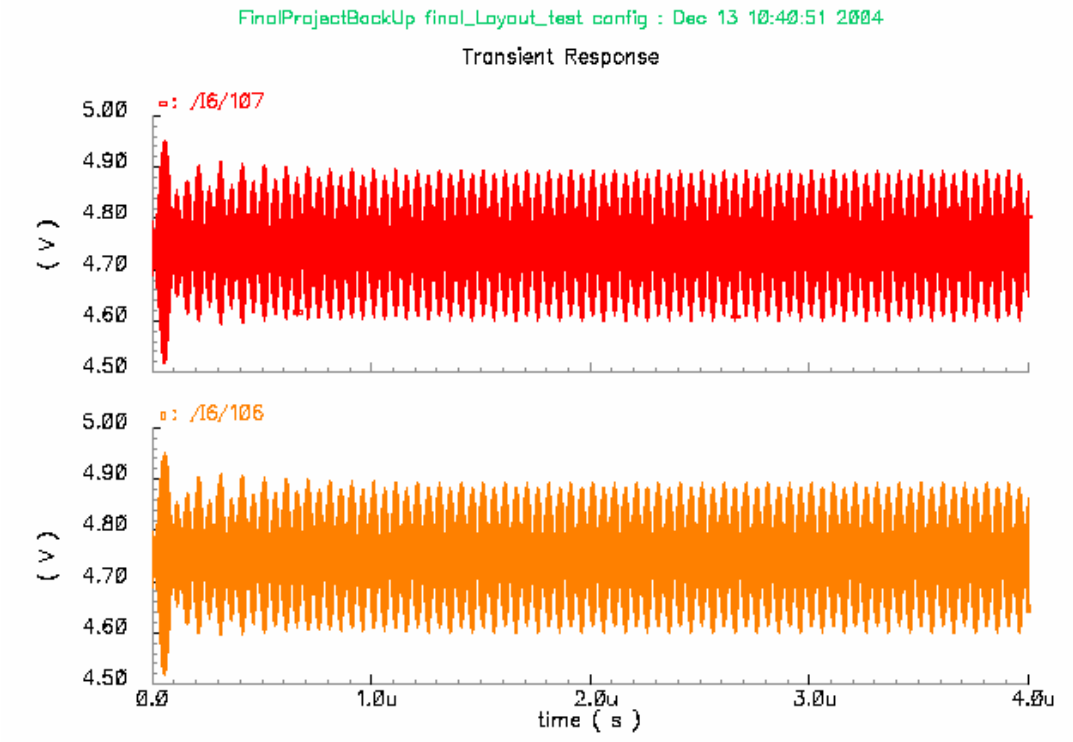

Fig. 5.2 Mixer's Differential Outputs

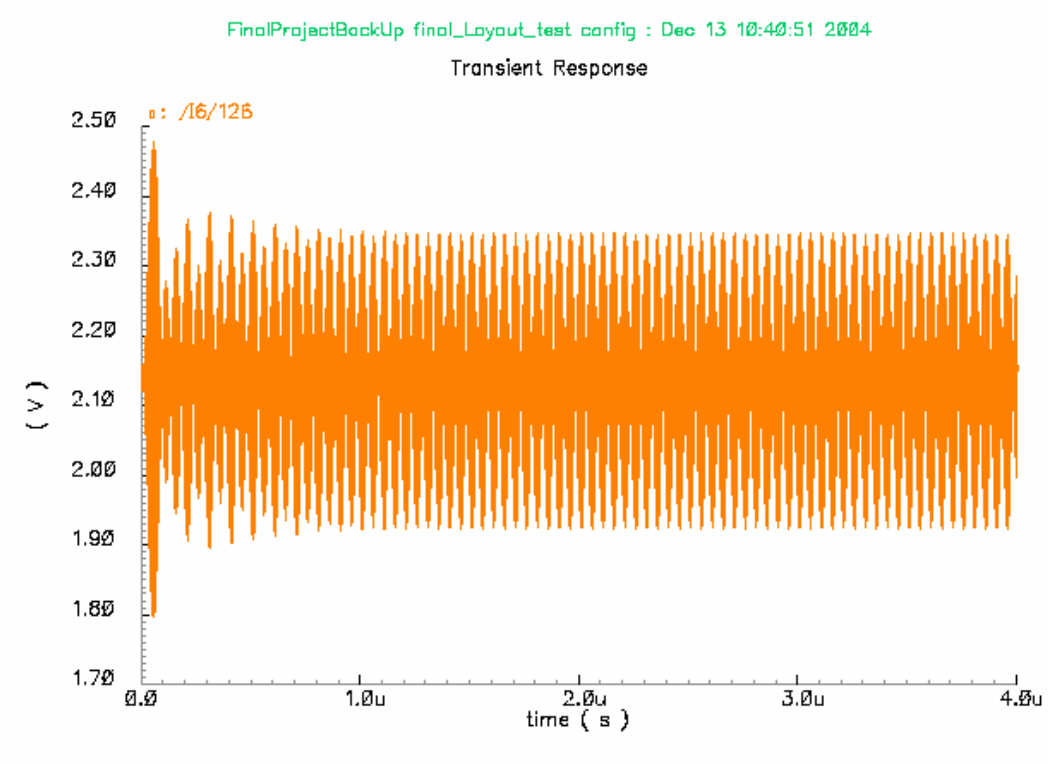

Fig. 5.3 Dif-to-Single Block Output

Mixer's two differential outputs fed to Dif-to-Single Block, which converts those two signals into single-ended version. The simulation result is shown in Fig. 5.3. Its Fourier Transform is given in Fig. 5.4.

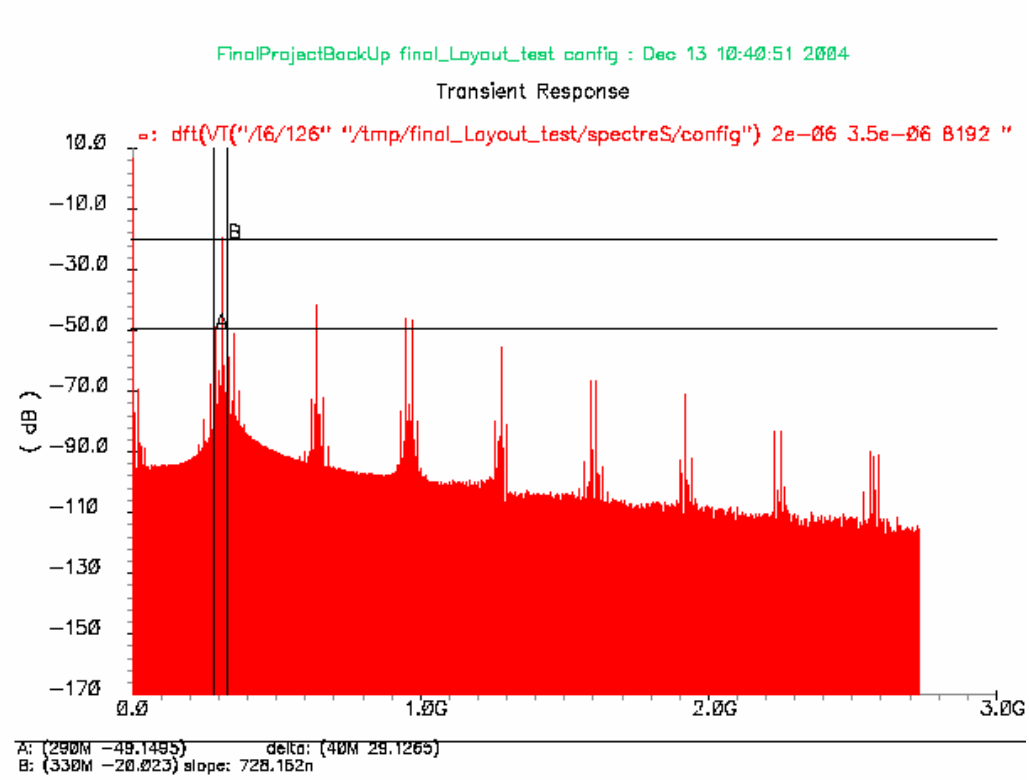

Fig. 5.4 Spectrum of Dif-to-Single Block Output

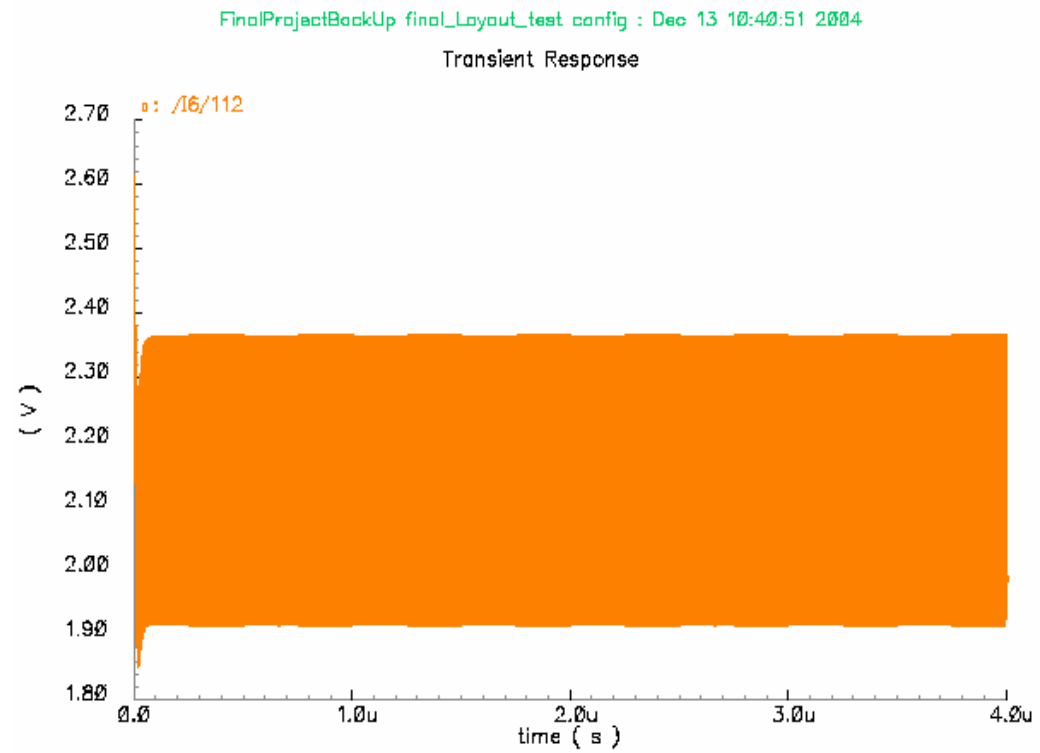

Fig. 5.5 LO_Input Macro Output

Fig. 5.5 shows the sine wave output of LO_Input Macro, its spectrum is give in Fig. 5.6.

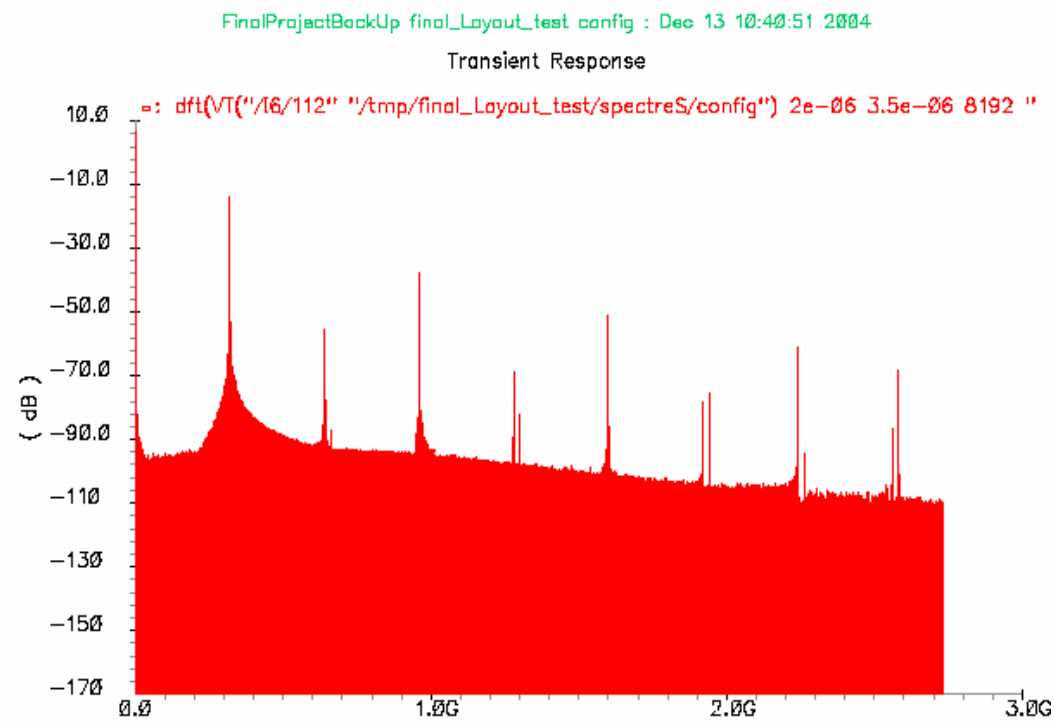

Fig. 5.6 Spectrum of LO_Input Macro Output

Fig. 5.7 shows the top level system simulation result. From this figure, we can see the FSK modulation scheme function properly.

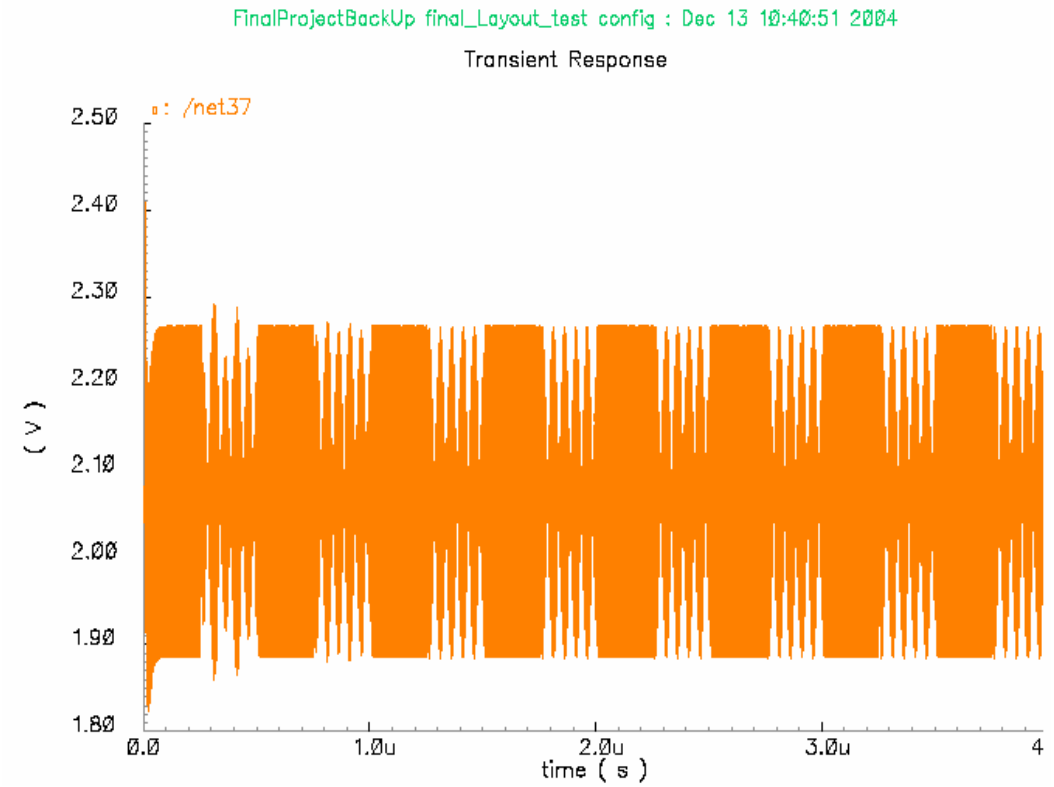

Fig. 5.7 Top Level Simulation Result

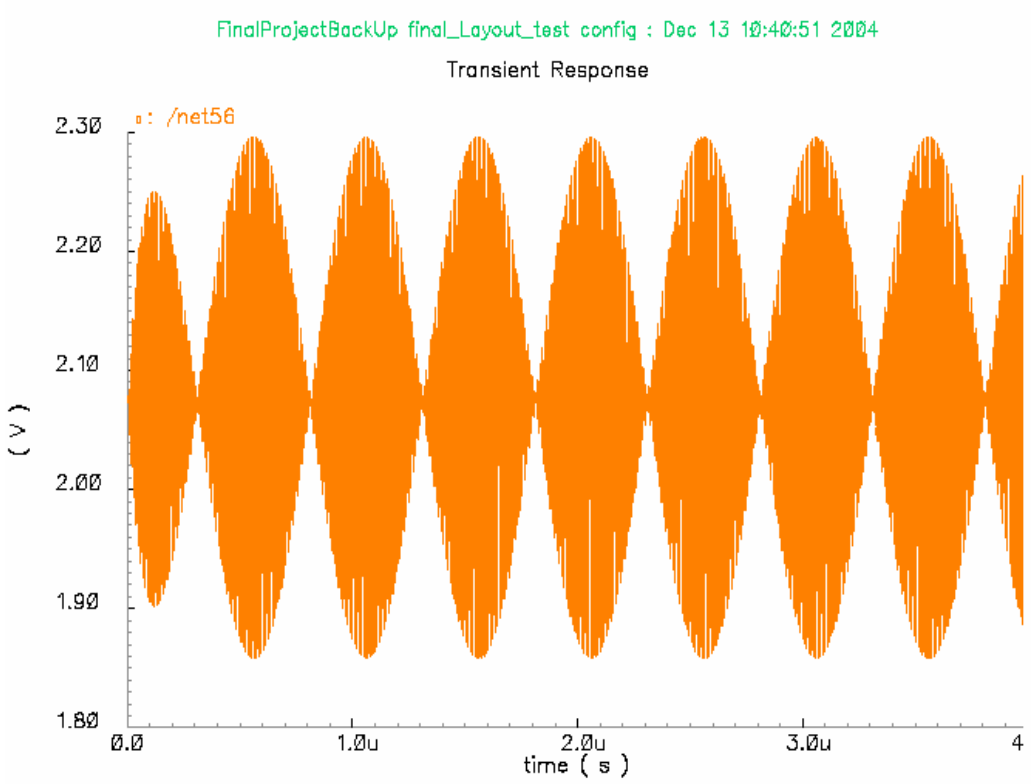

Fig. 5.8 Testing Result

This mixer can be used to mix signals of other frequencies. Fig. 5.8 gives an example in which IF frequency is 1MHz and LO signal is 100MHz. In the testing stage, other frequency can be tried.

6 Conclusions

In this project, a 320MHz upconverting mixer is designed. The post-layout simulation shows that this mixer works properly. Some extra circuits, such as single-to-differential circuit also shows correct function, which could be used in the future design. There is a design defect. The transistor ratio in the current source of the mixer is smaller than that of hand calculation. But still, the output current is around 5mA.

6.1 Future work

In this design, there are several current sources designed for different blocks, which is not necessary. In the future design, those current sources could be combined to save area and power consumption. The current source used in the mixer can be improved by using other kinds of structures, such as cascade or Wilson current source. In this design, analog buffer -3dB bandwidth is larger than 330MHz. But at 330MHz, the analog buffer's gain is less than one and has a large slope. In the future design, it's better to use wide bandwidth analog buffer.The magnitude of LO and IF signals can be chosen smaller than those in this design [6] to reduce feed-through and noise degradation. The layout could be further optimized so reduce area and parasitic parameters. It is better to use SpectreRF tool based on corresponding RF model to design mixer to give a better performance measurements.

Appendix A Schematics

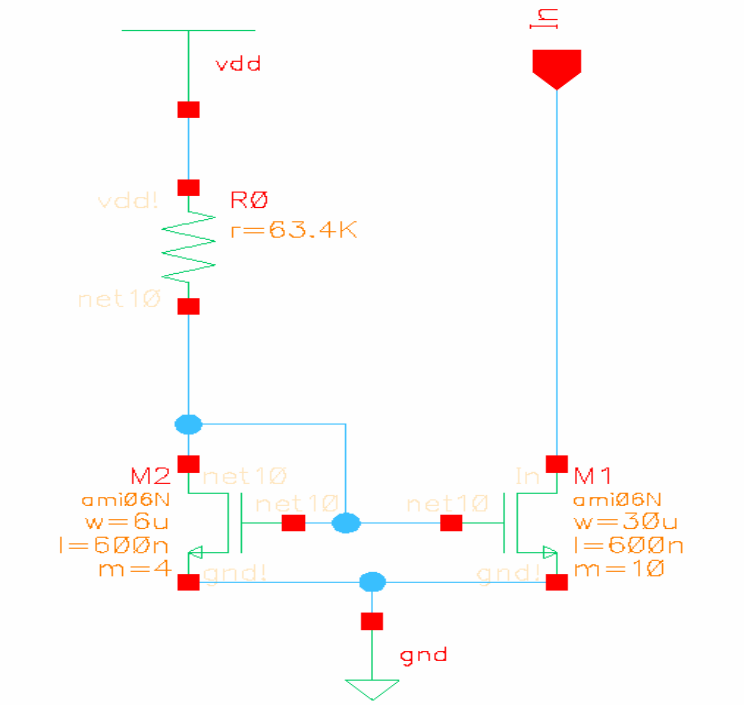

Fig. A.1 Current Source in the Mixer

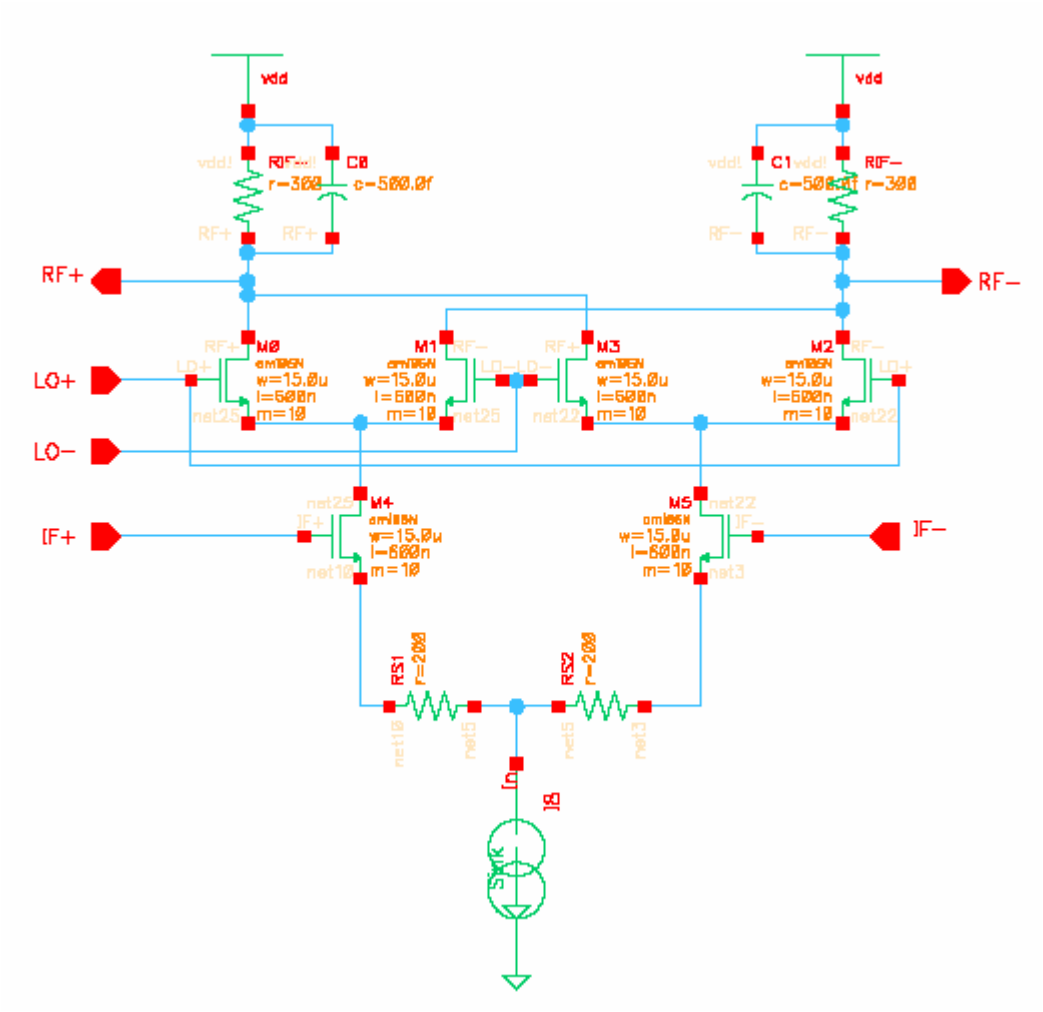

Fig. A. 2 Mixer Schematic

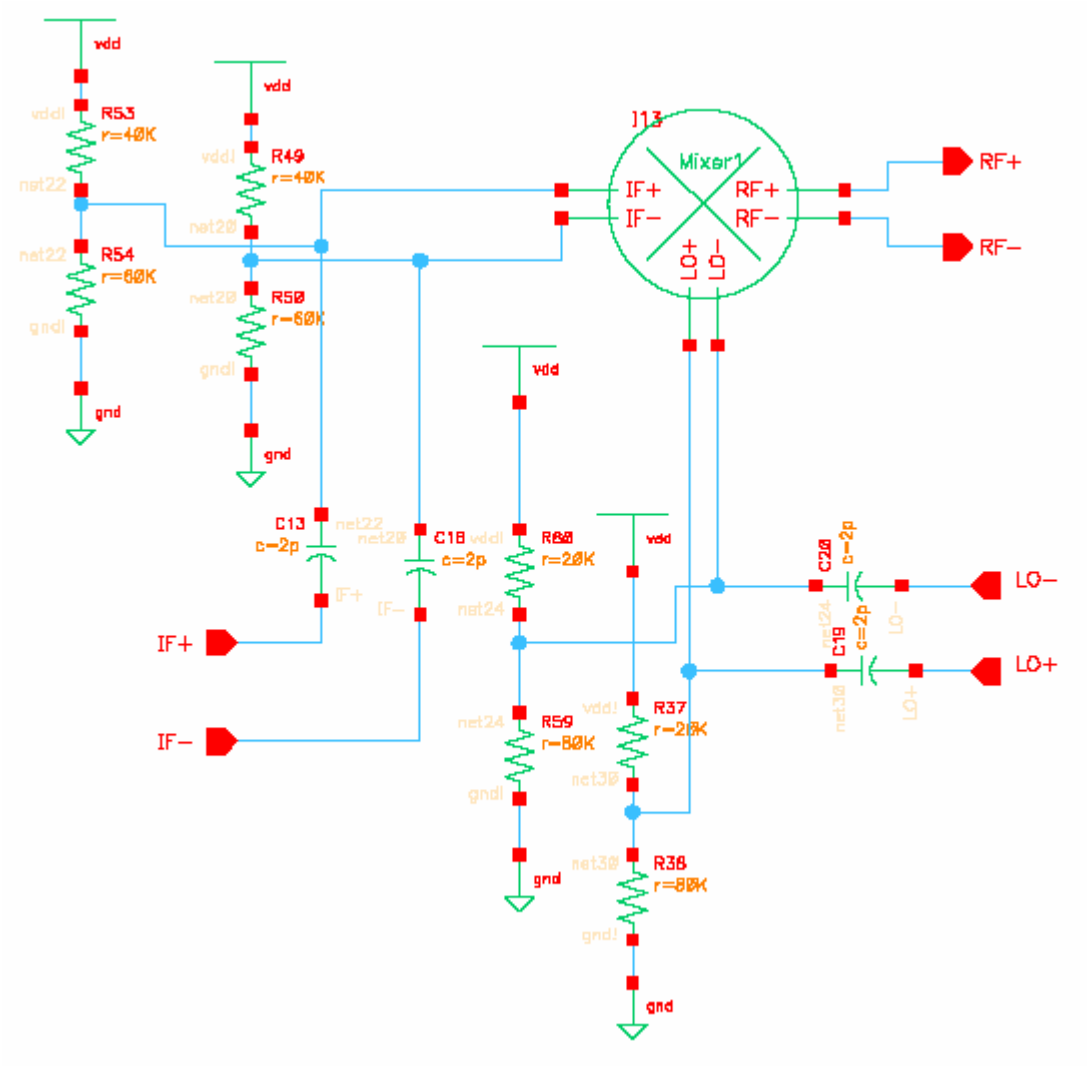

Fig. A.3 Mixer with Biasing Network

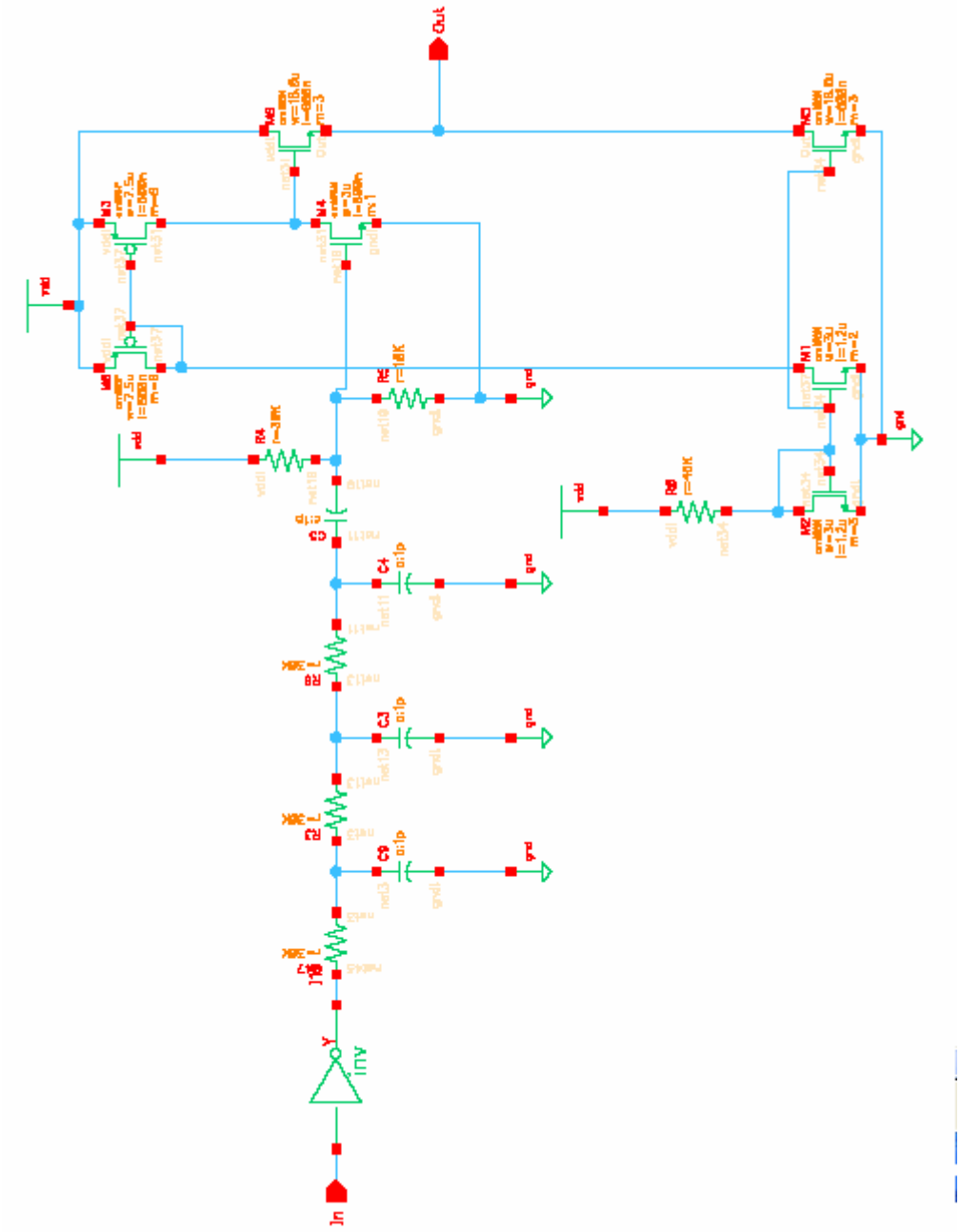

Fig. A.4 IF_Input Macro

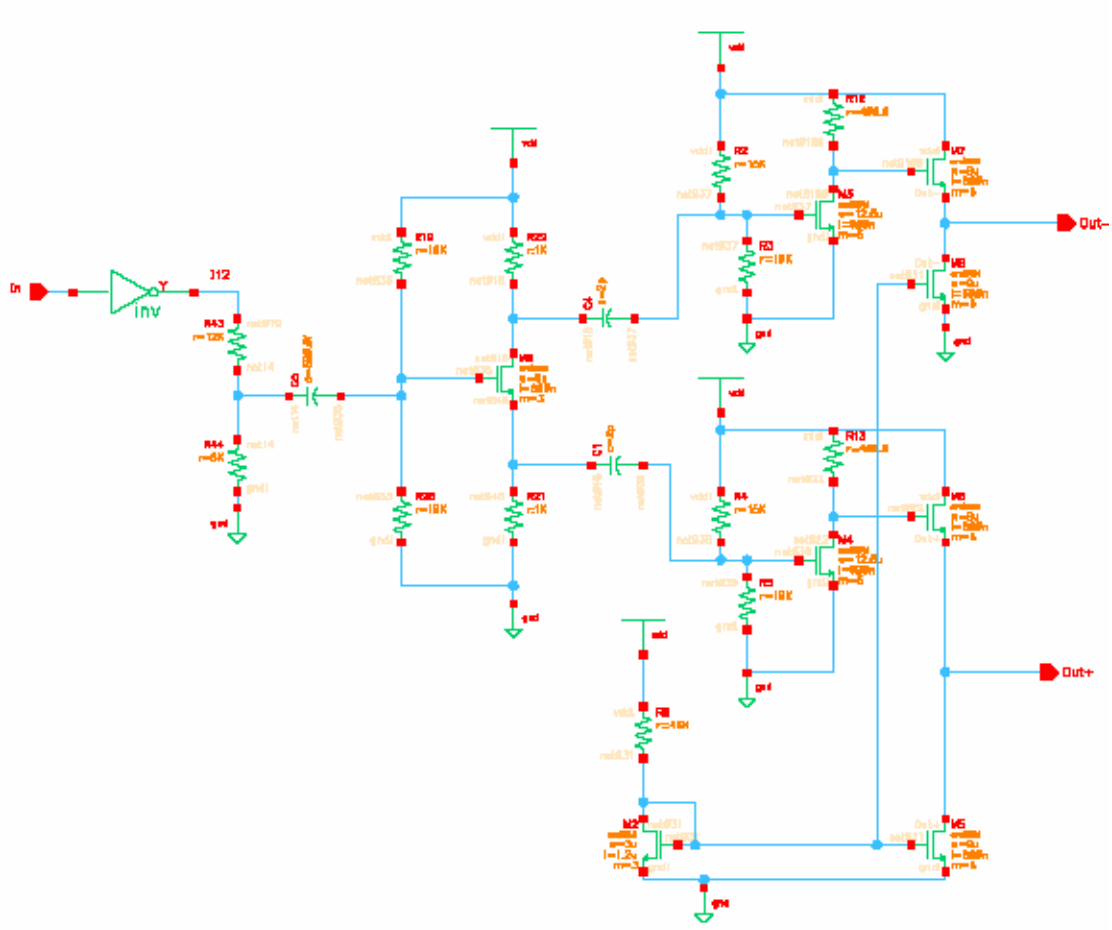

Fig. A. 5 Single-to-Differential Converter

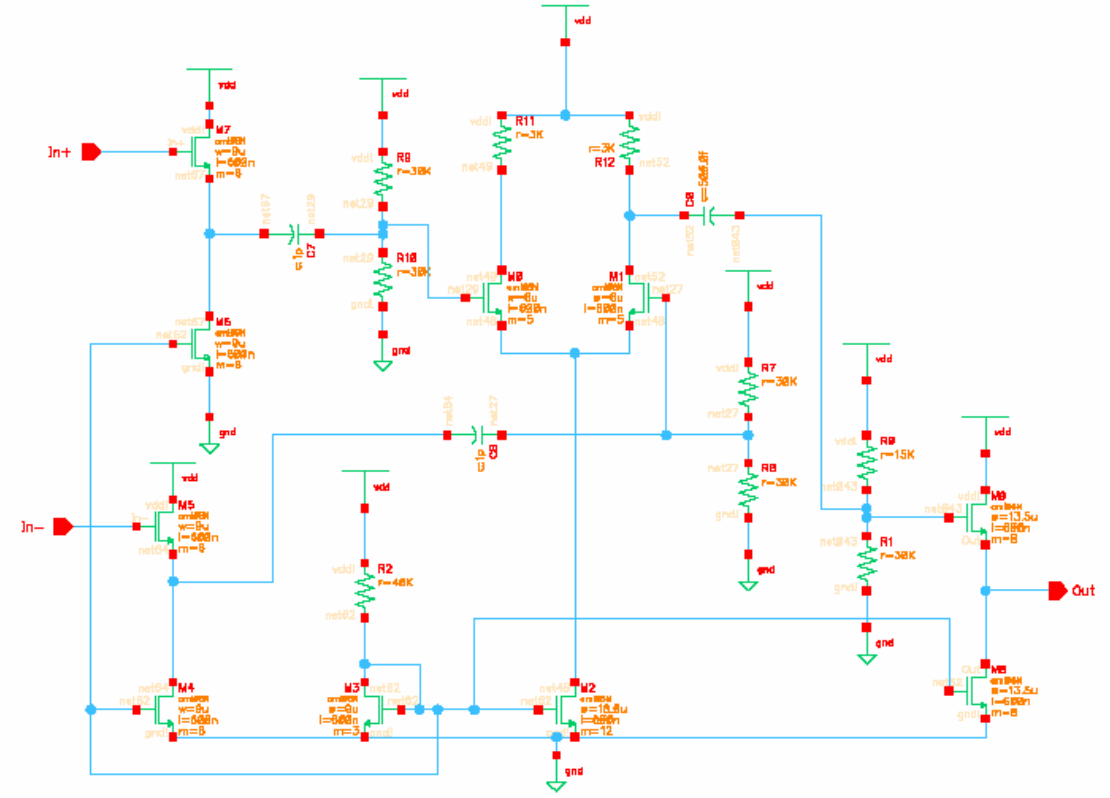

Fig. A. 6 Dif-to-Single Converter

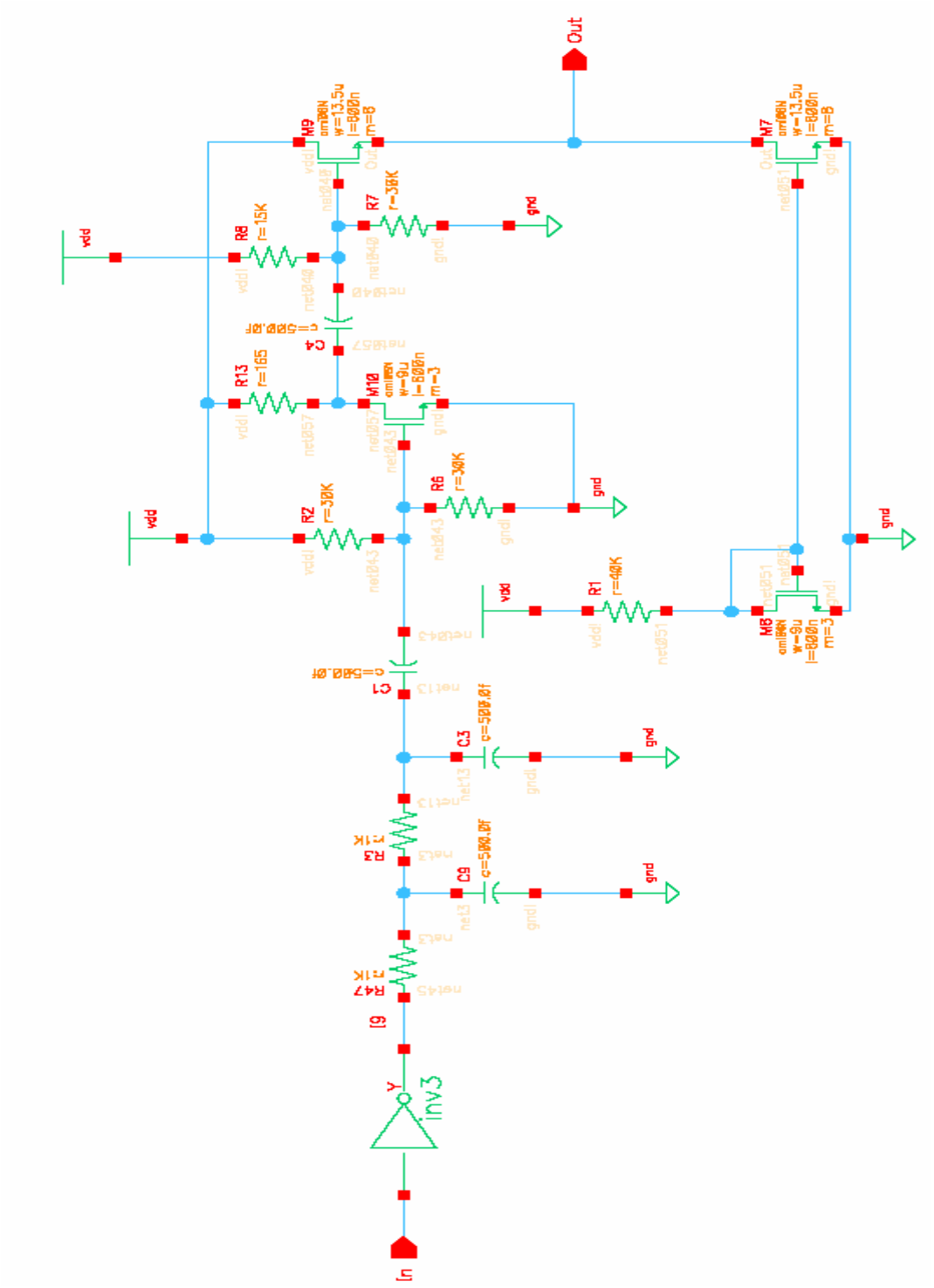

Fig. A.7 LO_Input Macro

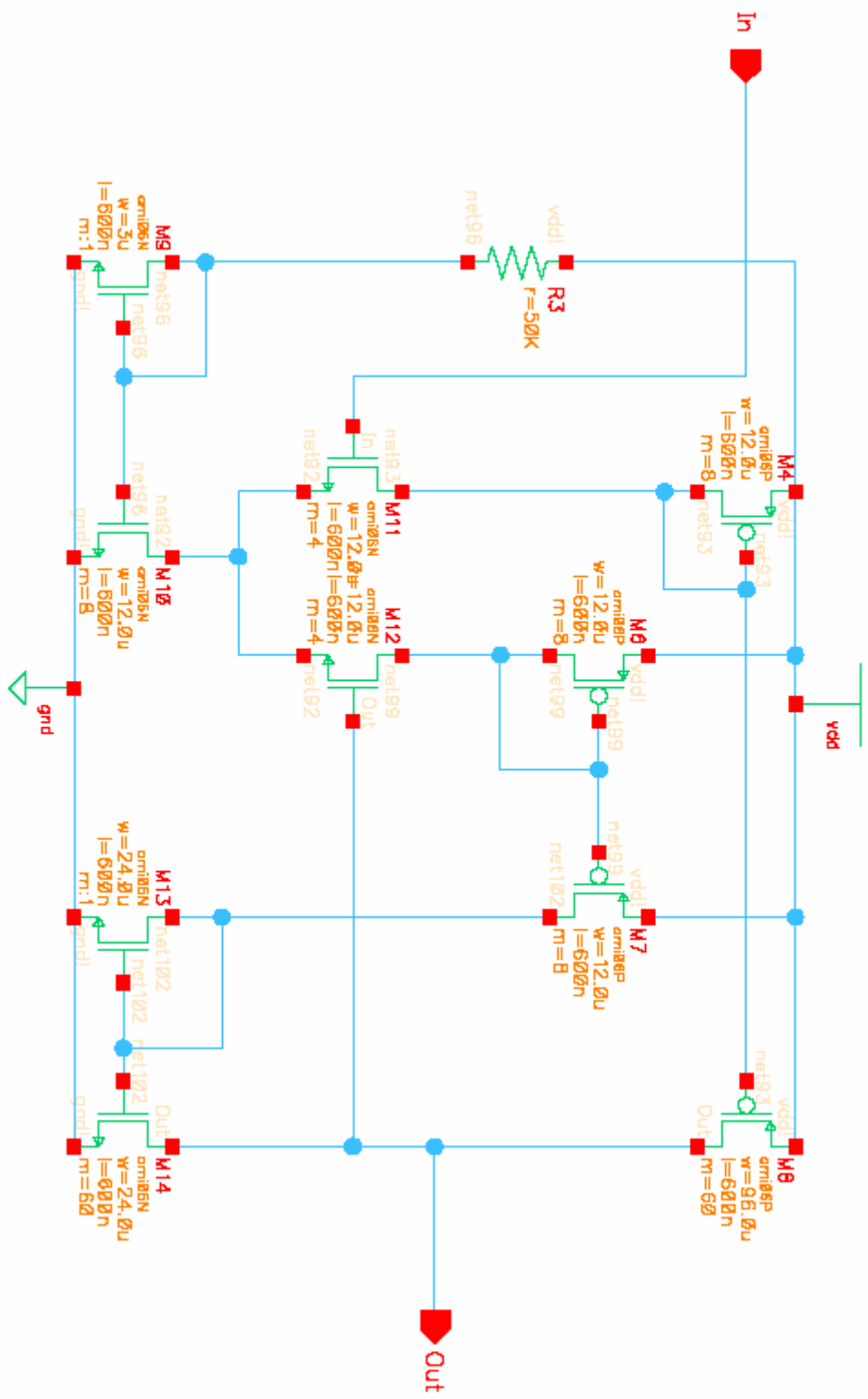

Fig. A.8 Analog Buffer

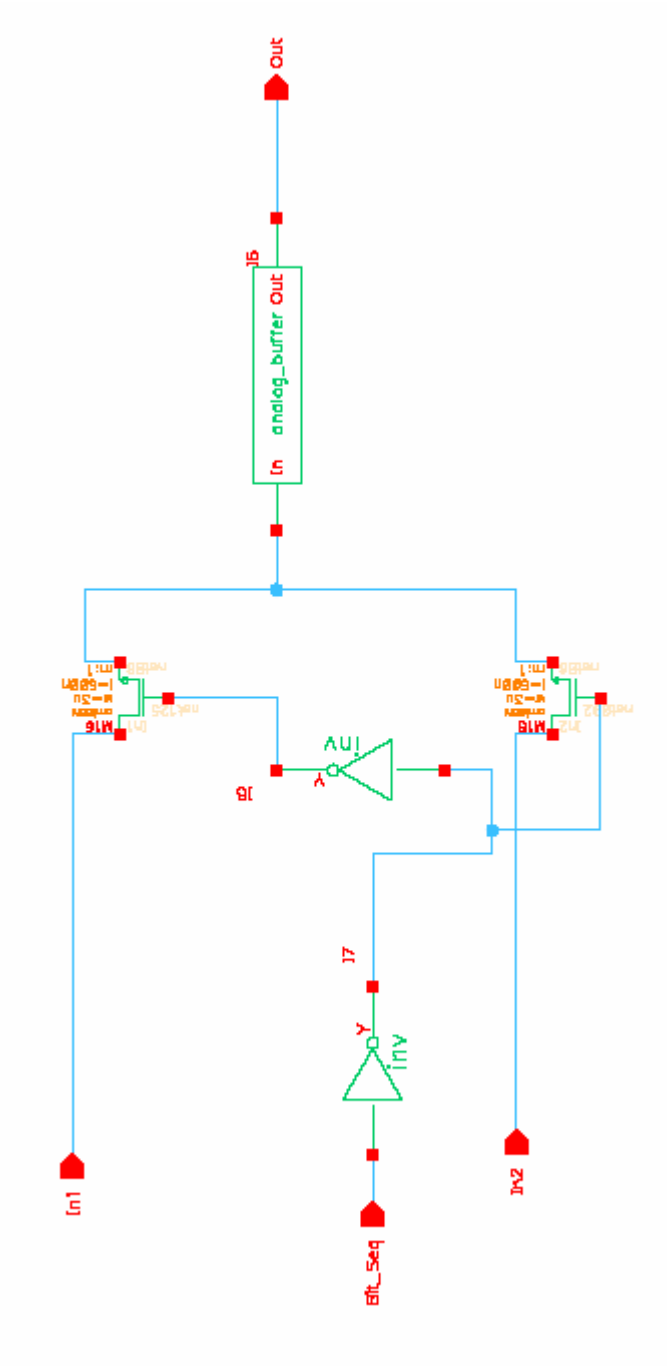

Fig. A.9 Modulator

Appendix B Layout

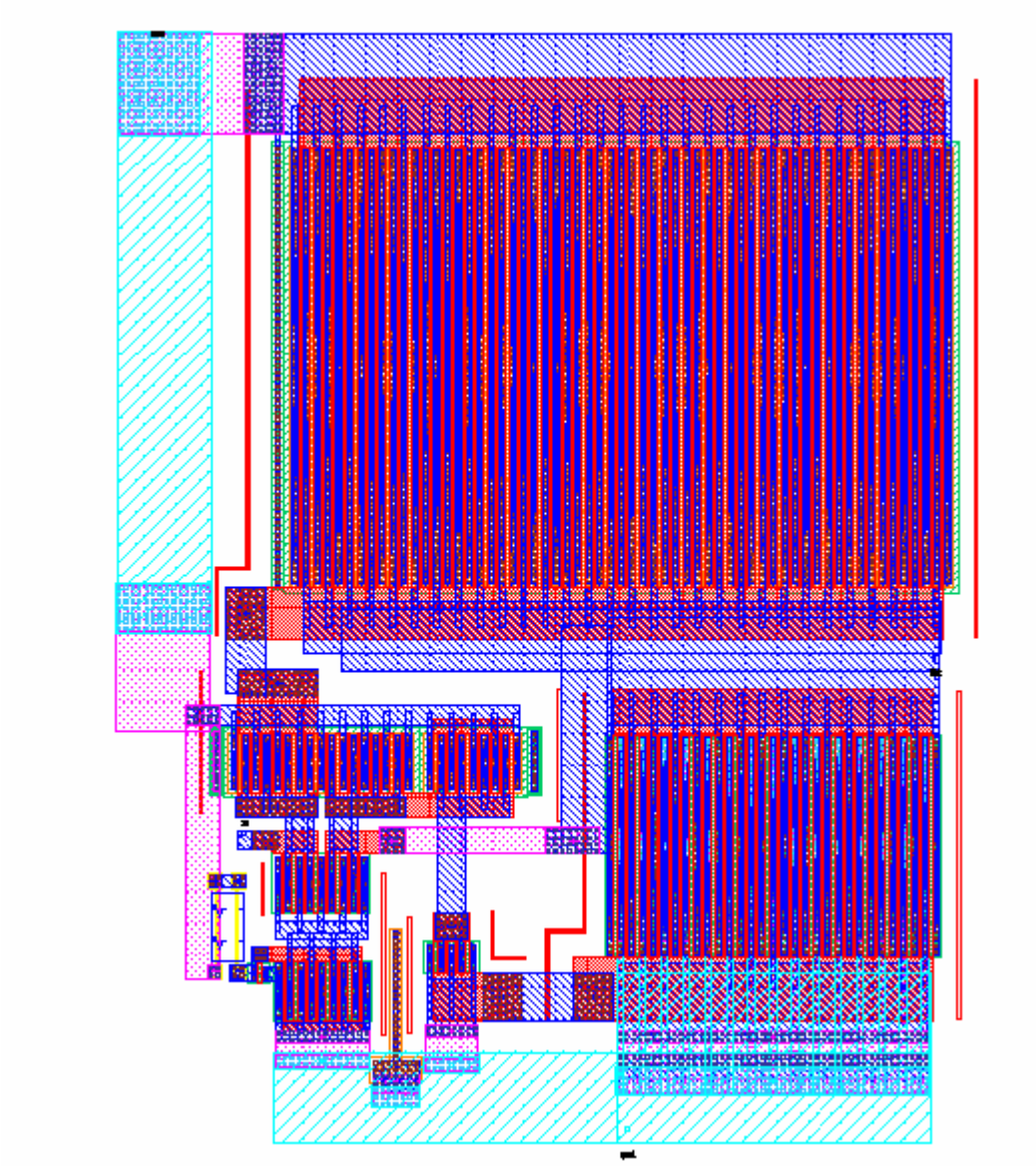

Fig. B.1 Analog Buffer

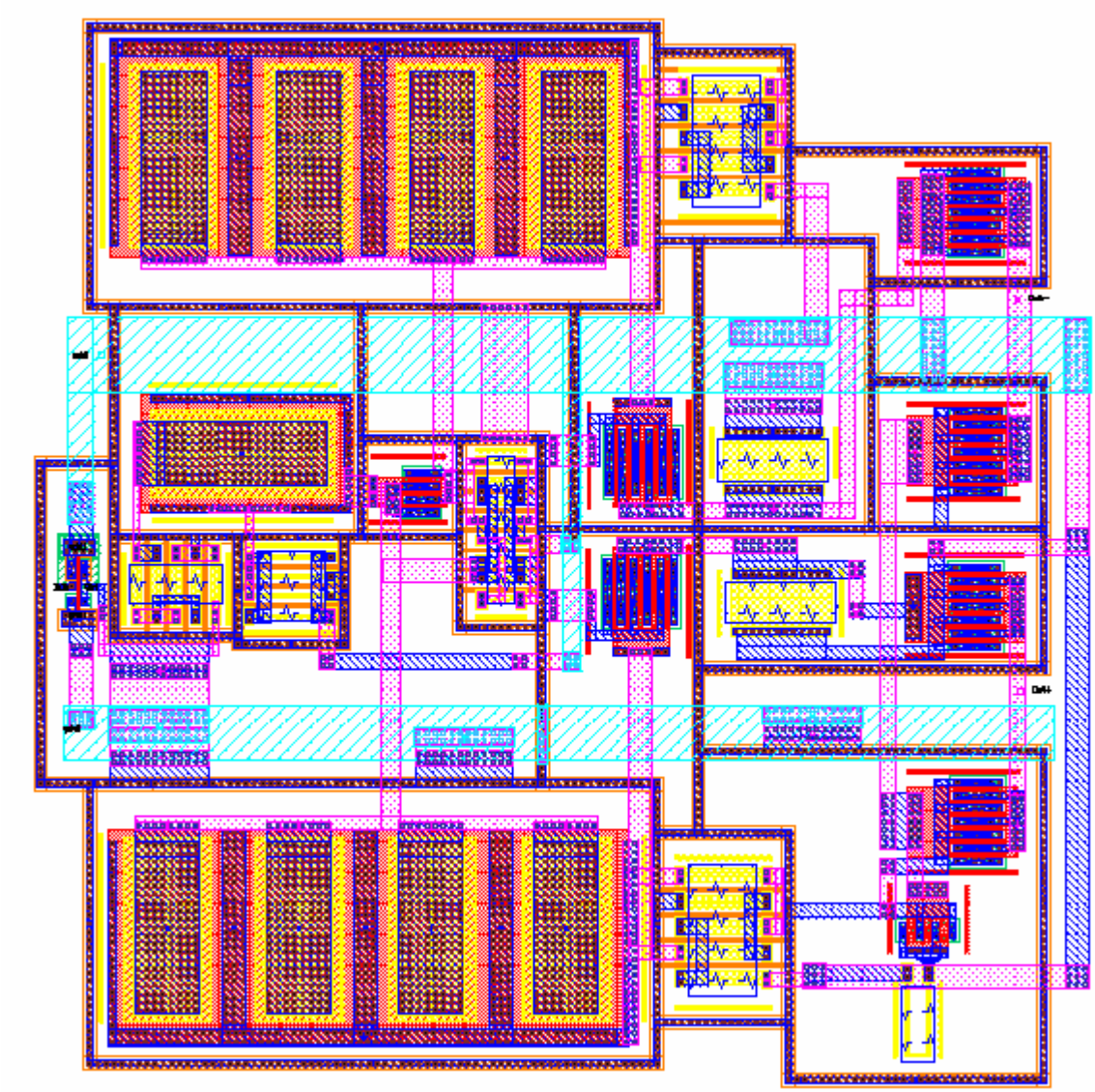

Fig. B.2 Single-to-Differential Converter

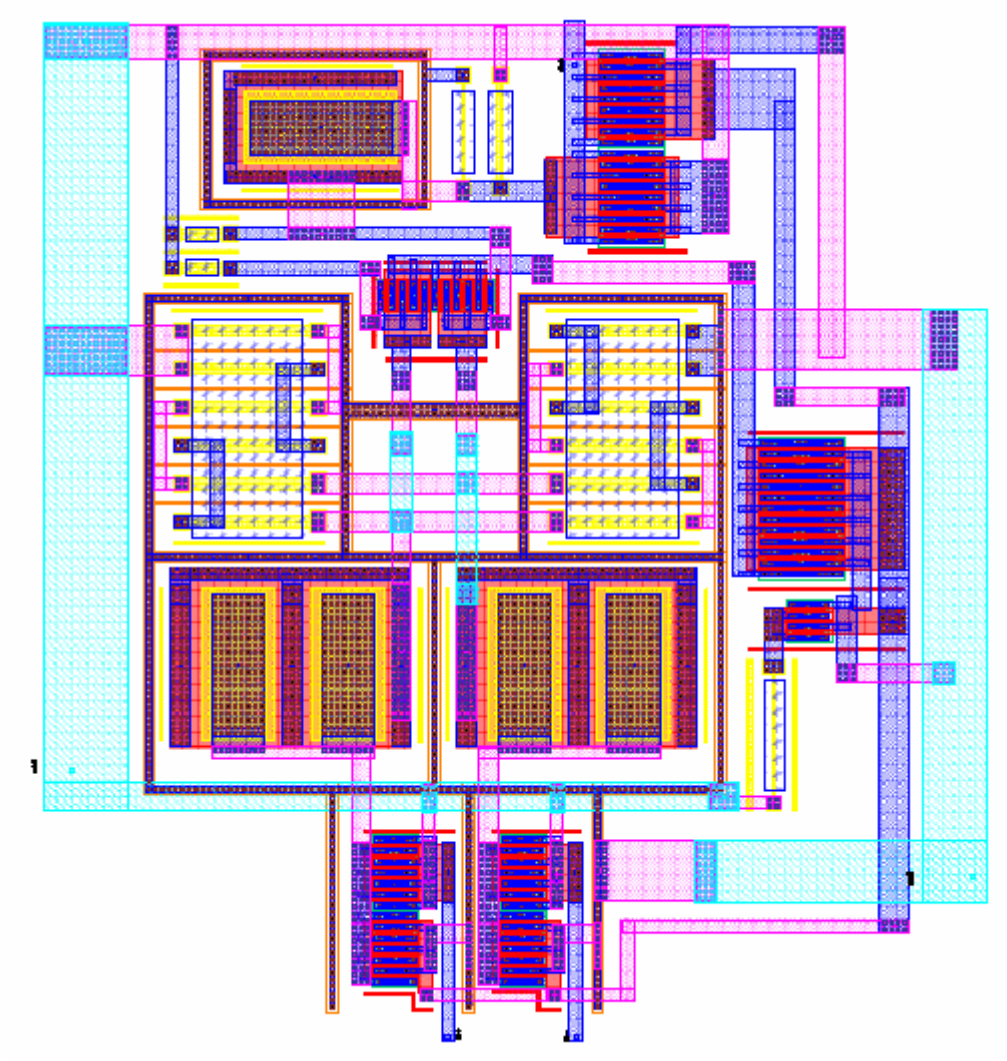

Fig. B.3 Dif-to-Single Converter

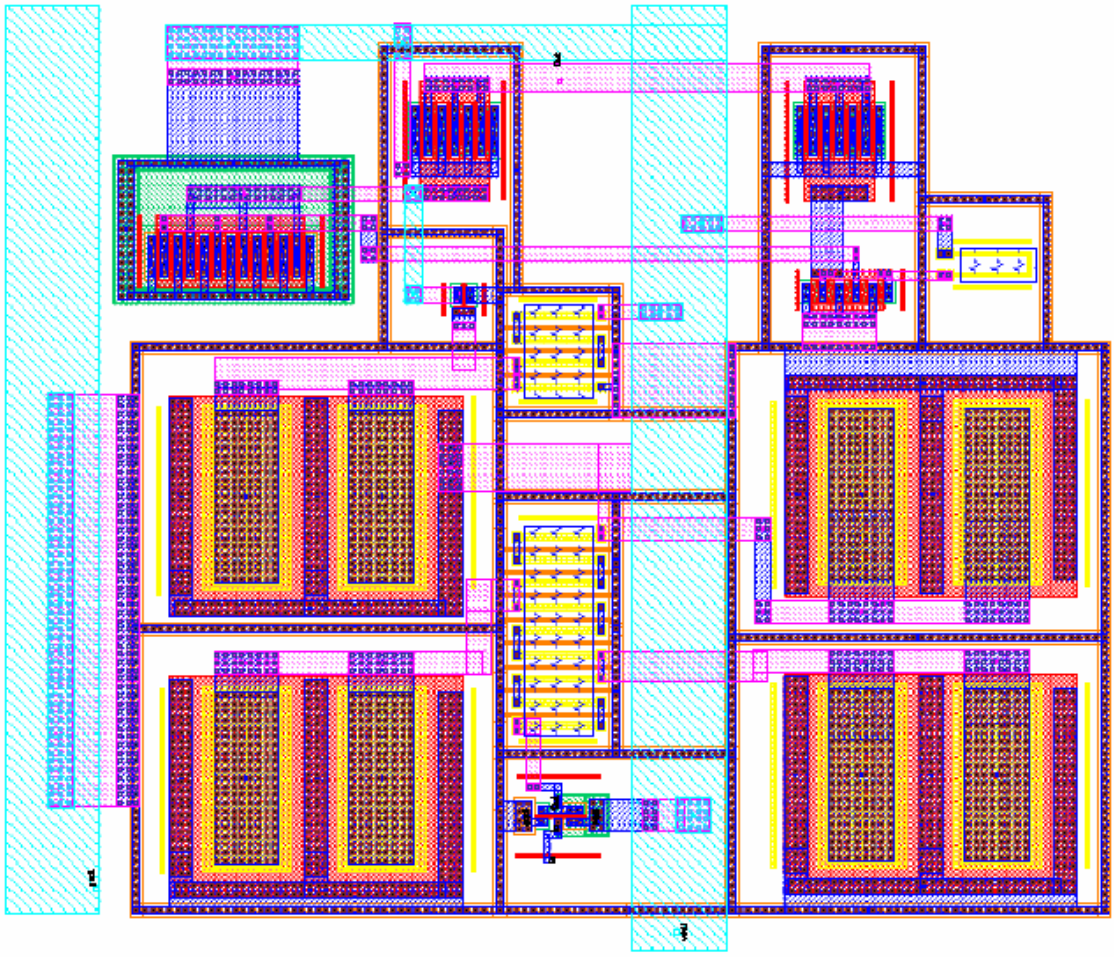

Fig. B.4 IF_Input Macro

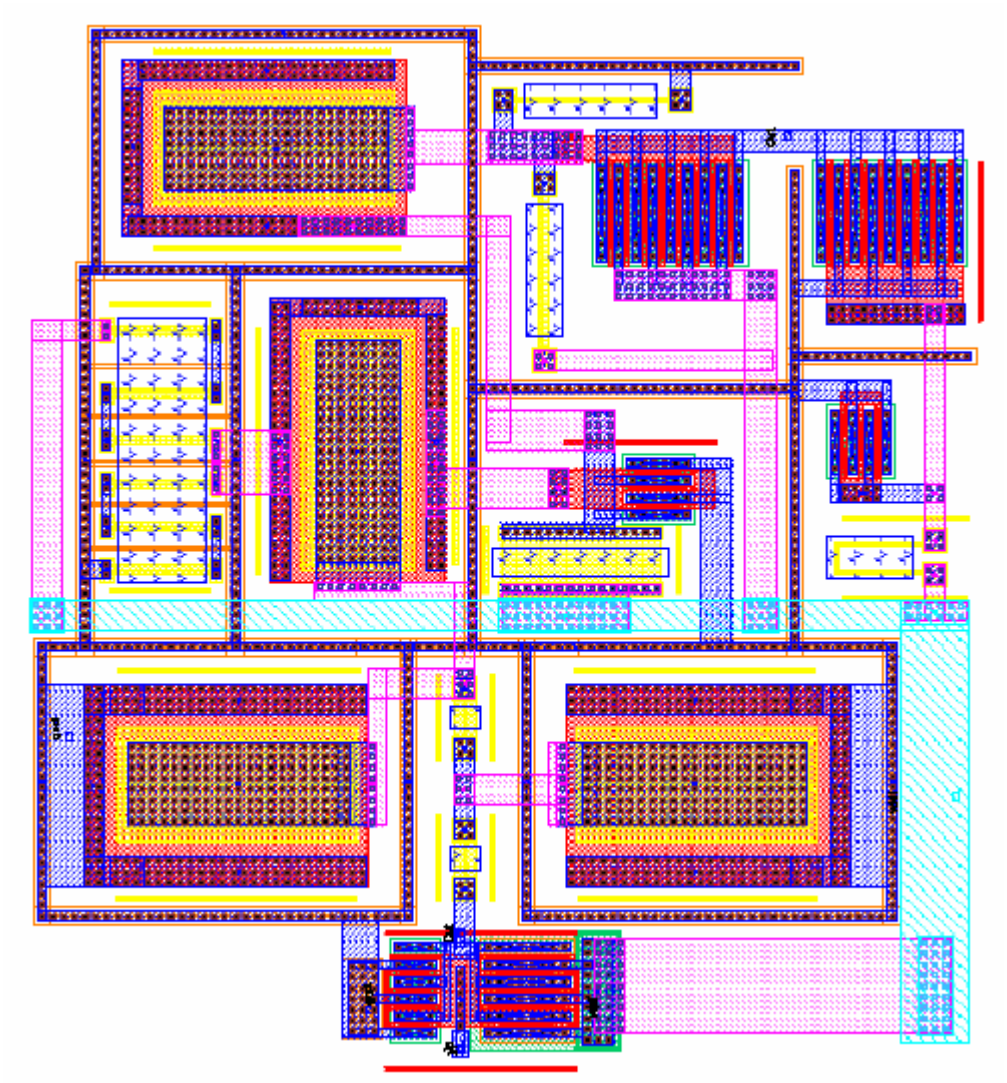

Fig. B.5 LO_Input macro

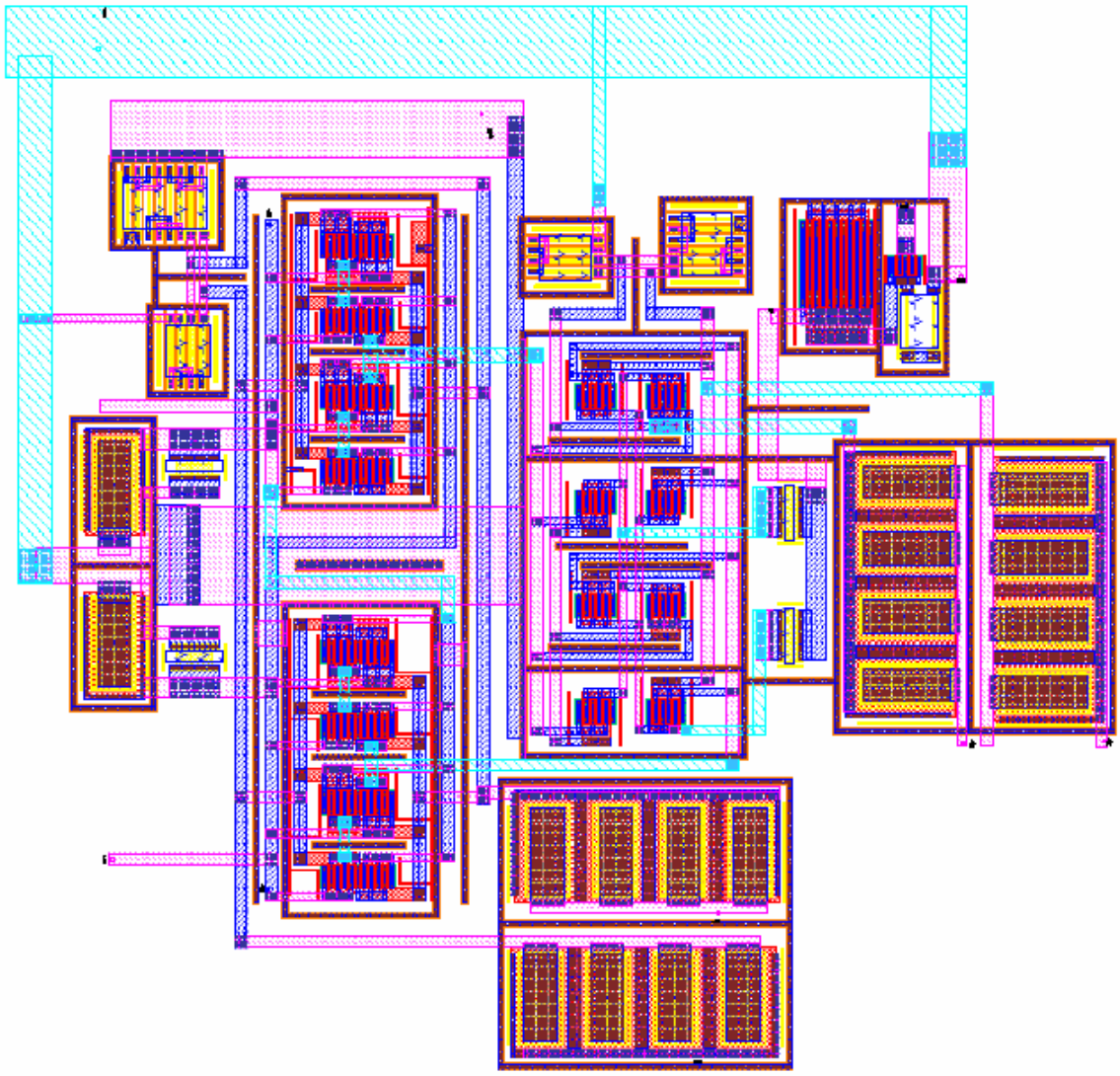

Fig. B. 6 Mixer with Biasing Network

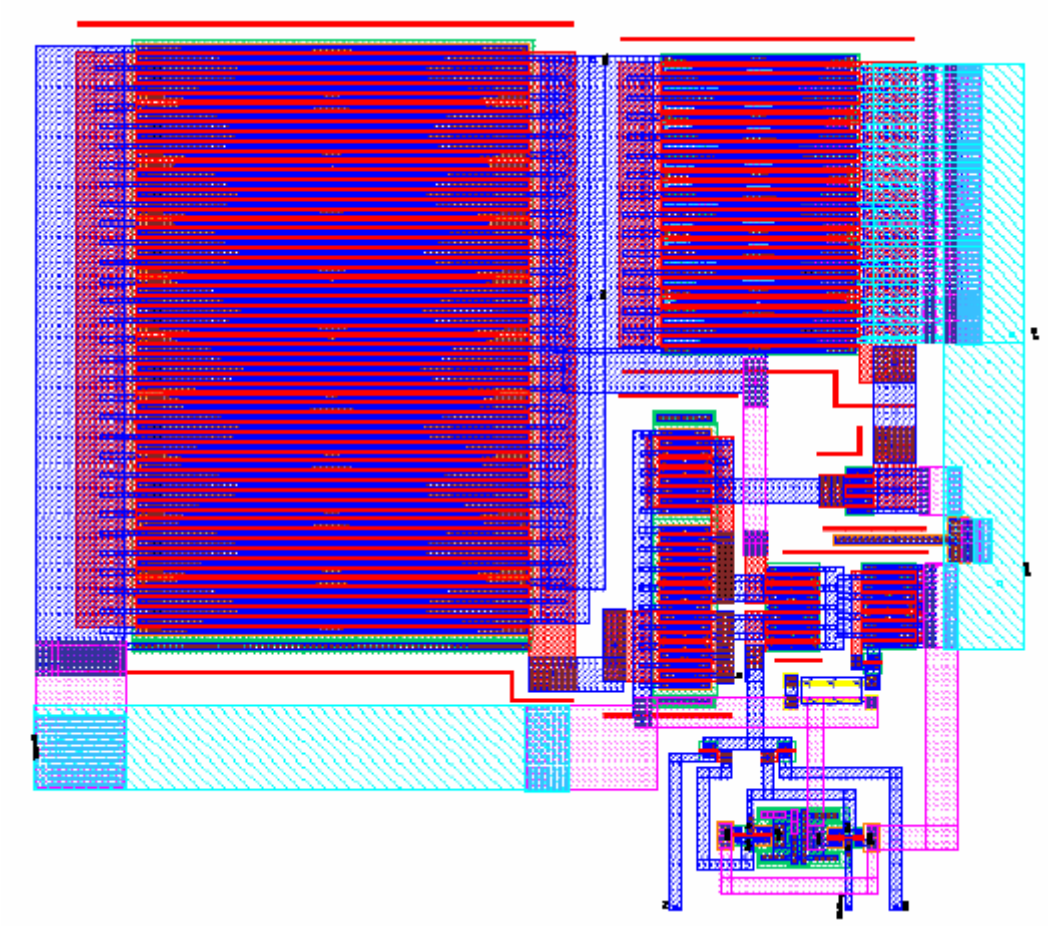

Fig. B.7 Modulator

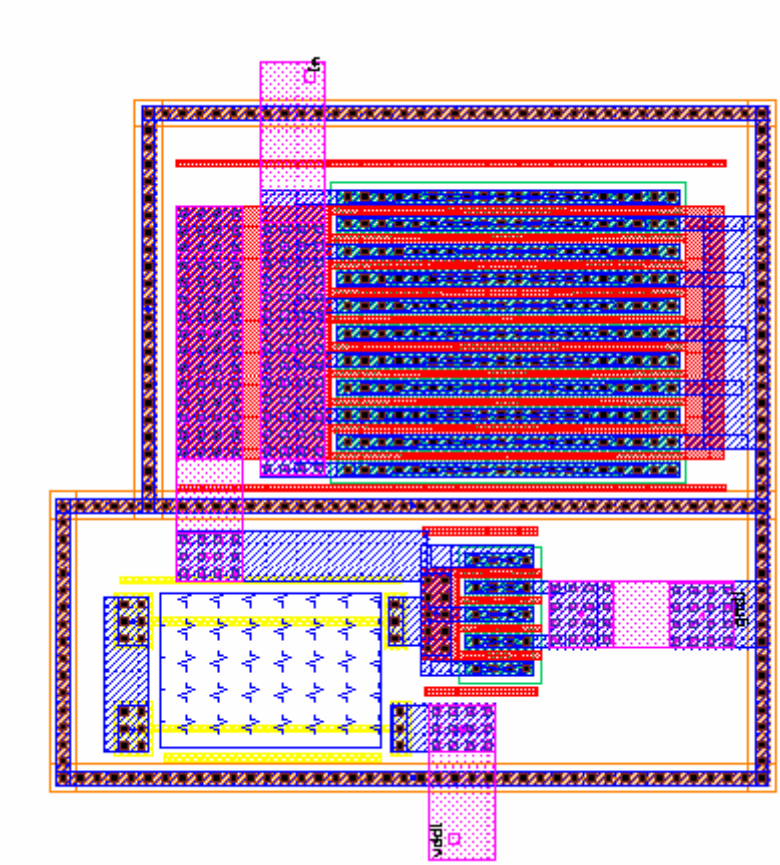

Fig. B.8 Current Sink

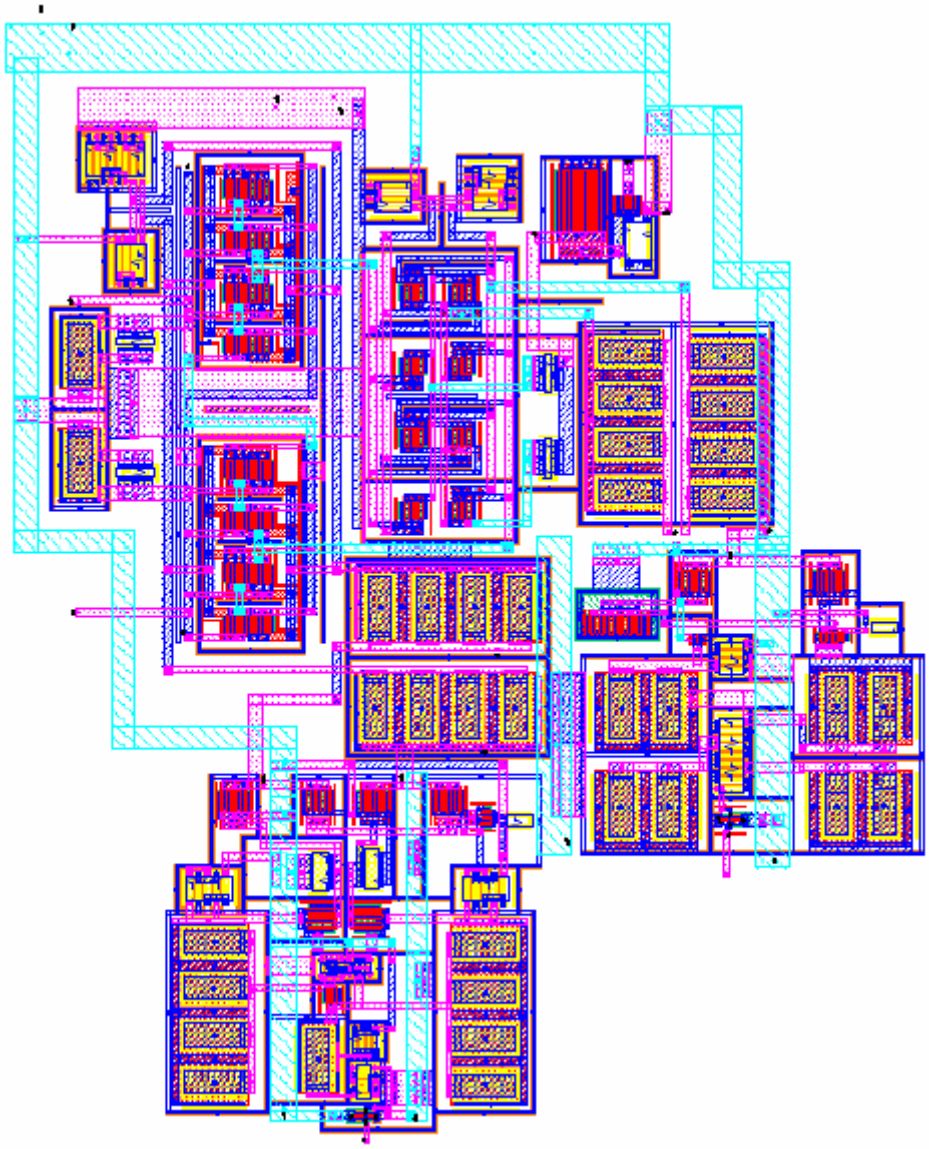

Fig. B.9 Upconverting Mixer

Acknowledgement

I’m grateful for the assistance got from Dr. Kotecki. He is always ready enough to help us, which makes the project design go smoothly. I also enjoy the discussions with my talented classmates, from whom I can always get help and insightful ideals.

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[4] Jan Crols et al., "A Single-Chip 900 MHz CMOS Receiver Front-End with a High Performance Low-IF Topology," IEEE J. Solid-State Circuits, Vol. 30, No. 12, Dec. 1995

[5] Paul R. Gray et al, Analysis and Design of Analog Integrated Circuits, 4th edition, John Wiley & Sons, Inc. 2001.

[6] John Rogers, Calvin Plett, Radio Frequency Integrated Cirtuit Design, Artech House Inc. 2003